APPLICATION		G01	REVISION		
NEXT ASSEMBLY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		PA	Release Per ECO #6687		

PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA																
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38

RECORD OF REVISION STATUS OF EACH SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES ANGLES ±

FRACTIONS ±

3 PLACE DECIMALS ±

2 PLACE DECIMALS ±

1 PLACE DECIMALS ±

MATERIAL:

CONTR NO.

DR	K McGrattan	9/27/90
CHK		
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APPROVED

BY DIRECTION OF

BBN Manufacturing Corporation

Billerica, MA

Drawing Title

TC/US TCS Slave Functional Specification

Size		Drawing No.
A	63942	FS19706G01
Scale		Sheet 1 of 23

TC/US TCS Slave Processor Firmware Specification

1.1 Introduction

The TC/US is the TC2000 unified switch card. It is equipped with a TC2000 Test and Control System (TCS) Slave Processor, a Motorola 68HC11 single chip microcomputer. This programmed device implements master/slave communication and circuit board control defined in the *TC2000 Technical Reference Guide*.

This document describes the commands defined for a TC/US Slave Processor. BBN programmed part number 4619706G01.

1.2 TCS Messages

There are four types of TCS message:

- Register Access Request
- TBUS Memory Access Set-Up Request
- TBUS Memory Read Request
- TBUS Memory Write Request

None of the TBUS messages are defined for the TC/US slave processor. Issuing a memory message to a TC/US results in a negative acknowledgement from the slave.

1.2.1 Slave Addressing

The TC/US slave is initialized to broadcast group 0x00. The slave will carry out requests broadcast to this group, but will not respond. An EEPROM register defines the slave's group, so it may be modified during operation.

1.3 Register Access Messages

There are four types of register access message:

Action Registers — Action registers perform a sequence of actions on the target circuit card; thus hiding board specific and 68HC11 details.

EEPROM Registers — EEPROM registers store board specific information in slave processor non-volatile memory.

Gate Array Registers — The gate array register messages access registers within the card's Switch Gate Arrays (SGAs).

Hardware Registers — Hardware write registers load board control registers. Hardware read registers monitor board status signals and data bits. A new type of hardware register access has been added to the TCUS. It is a hardware shadow register read only access. Hardware shadow read registers return the shadow copy of the board control registers.

1.4 Command Byte Decoding

Cmd Type, Cmd Mod		Description
Memory Messages		
0,1	Don't Care	Illegal Commands
Memory Set-Up Message		
2,3	Don't Care	Illegal Commands
Register Access Messages		
Action Registers		
4	Don't Care	Action Register Read (See List of Action Registers)
5	Don't Care	Action Register Write (See List of Action Registers)
EEPROM Registers		
6	Don't Care	EEPROM Register Read (See EEPROM Register List)
7	Don't Care	EEPROM Register Write (See EEPROM Register List)
Gate Array Registers		
8	0	Read TC/US SGA #0 Registers
	1	Read TC/US SGA #1 Registers
	2	Read TC/US SGA #2 Registers
	3	Read TC/US SGA #3 Registers
	4-15	Illegal Commands
9	0	Write TC/US SGA #0 Registers
	1	Write TC/US SGA #1 Registers
	2	Write TC/US SGA #2 Registers
	3	Write TC/US SGA #3 Registers
	4-15	Illegal Commands
Hardware Registers		
10	0	Read Hardware Register 0
	1	Read Hardware Register 1
	2	Read Hardware Register 2
	3	Read Hardware Register 3
	4-15	Illegal Commands
11	0	Write Hardware Register 0
	1	Write Hardware Register 1
	2	Write Hardware Register 2
	3	Write Hardware Register 3
	4	Write Hardware Register 4
	5-15	Illegal Commands
Shadow Registers		
12	0	Read Hardware Shadow Register 0
	1	Read Hardware Shadow Register 1
	2	Read Hardware Shadow Register 2
	3	Read Hardware Shadow Register 3
	4	Read Hardware Shadow Register 4
	5	Read Shadow Register 5
	6	Read Shadow Register 6
	7	Read Shadow Register 7
	8	Read Shadow Register 8
	9	Read Shadow Register 9
	10	Read Shadow Register 10
	11	Read Shadow Register 11

	12	Read Shadow Register 12
	13	Read Shadow Register 13
	14	Read Shadow Register 14
	15	Read Shadow Register 15
13	0	Write Hardware Shadow Register 0
	1	Write Hardware Shadow Register 1
	2	Write Hardware Shadow Register 2
	3	Write Hardware Shadow Register 3
	4	Write Hardware Shadow Register 4
	5	Write Shadow Register 5
	6	Write Shadow Register 6
	7	Write Shadow Register 7
	8	Write Shadow Register 8
	9	Write Shadow Register 9
	10	Write Shadow Register 10
	11	Write Shadow Register 11
	12	Write Shadow Register 12
	13	Write Shadow Register 13
	14	Write Shadow Register 14
	15	Write Shadow Register 15

1.5 Action Register List

The TCS message's address byte selects which register is accessed.

The TCS message's data byte is unused in the read message, and conveys write data in the write message.

Reg. Number		Description	Read/Write
0	(0x00)	Board Status Register	(read only)
1	(0x01)	Card Control Register	(write only)
2	(0x02)	Power Control Register	(write only)
3	(0x03)	Previous ACK/NACK	(read only)
4	(0x04)	Clock Activity Check Register	(read only)
5	(0x05)	EEPROM Write Enable	(write only)
6	(0x06)	Temperature near SGA #1 & #3	(read only)
7	(0x07)	Execute Clear and Test RAM	(read/write)
8	(0x08)	Slave Address Re-Read Command	(write only)
9	(0x09)	Illegal Command	(n/a)
10	(0x0A)	Illegal Command	(n/a)
11	(0x0B)	-4.5 VDC Voltage Level (Vee)	(read only)
12	(0x0C)	-2 VDC Voltage Level (Vtt)	(read only)
13	(0x0D)	LED Control	(write only)
14	(0x0E)	Illegal Command	(n/a)
15	(0x0F)	Illegal Command	(n/a)
16	(0x10)	Illegal Commnad	(n/a)
17	(0x11)	Temperature near SGA #0 & #2	(read only)
18	(0x12)	Illegal Command	(n/a)
19	(0x13)	SGA #0 -3.8 VDC Voltage Level	(read only)
20	(0x14)	SGA #1 -3.8 VDC Voltage Level	(read only)
21	(0x15)	Illegal Command	(n/a)
22	(0x16)	Illegal Command	(n/a)
23	(0x17)	Illegal Commnad	(n/a)
24	(0x18)	Illegal Commnad	(n/a)
25	(0x19)	Illegal Command	(n/a)
26	(0x1A)	Illegal Command	(n/a)

1.6 EEPROM Register List

Reg. Number		Description	Read/Write
0	(0x00)	Card Type	(read/write)
1-16	(0x01-10)	Serial Number	(read/write)
17,18	(0x11,12)	Artwork Revision Level	(read/write)
19,20	(0x13,14)	Electrical Revision Level	(read/write)
21,22	(0x15,16)	TCS Slave Code Revision Level	(read/write)
23	(0x17)	Temperature Alarm Setpoint	(read/write)
24	(0x18)	TCS 5 VDC Nominal A/D Reading	(read/write)
25	(0x19)	-4.5 VDC Nominal A/D Reading	(read/write)
26	(0x1A)	-2 VDC Nominal A/D Reading	(read/write)
27	(0x1B)	SGA 0 -2 VDC Nominal Reading	(read/write)
28	(0x1C)	SGA 1 -2 VDC Nominal Reading	(read/write)
29	(0x1D)	Reserved for TEX	(read/write)
30	(0x1E)	Reserved for TEX	(read/write)
31	(0x1F)	Card Group ID for broadcasts	(read/write)

1.7 Hardware Register List

Hardware registers are selected between with the TCS message command modifier field. The TCS message address byte is not used by hardware register accesses.

Reg. Number		Description	Read/Write
Write Registers			
0	(0x00)	Margin, Monitor, and LED control	(write only)
1	(0x01)	Margin Disable, Power Enable, and TCS Path Enable <9..8>	(write only)
2	(0x02)	TCS Path Enable <7..0>	(write only)
3	(0x03)	Gate Array Execute Lines, RAND Control, and SGA Reset	(write only)
4	(0x04)	Net Time Control	(write only)
Read Hardware Registers			
0	(0x00)	Status<2..0> and Bay ID<2>	(read only)
1	(0x01)	Bay ID<1..0> and Midplane ID<2..1>	(read only)
2	(0x02)	Midplane ID<0> and Slot ID<2..0>	(read only)
3	(0x03)	Card Type <3..0>	(read only)

1.8 Hardware Shadow Register List

Hardware Shadow registers are selected using the TCS message command modifier field. The TCS message address byte is not used by hardware shadow register accesses. Hardware Shadow register access is read/write. **Note that the Hardware Shadow registers can be written independently of the actual Hardware registers. If this is done, it can lead to inconsistencies between the state of the actual TCUS board and the slaves knowledge of the TCUS board. As the actual Hardware registers do not have readback capability, this can be fatal. Program these registers with caution.**

Reg. Number		Description	Read Only
Read Hardware Shadow Registers			
0	(0x00)	Margin, Monitor, and LED control	(read/write)
1	(0x01)	Margin Disable, Power Enable, and TCS Path Enable <9..8>	(read/write)
2	(0x02)	TCS Path Enable <7..0>	(read/write)
3	(0x03)	Gate Array Execute Lines, RAND Control, and SGA Reset	(read/write)
4	(0x04)	Net Time Control	(read/write)
5	(0x05)	Reserved for TEX	(read/write)
6	(0x06)	Reserved for TEX	(read/write)
7	(0x07)	Reserved for TEX	(read/write)
8	(0x08)	Reserved for TEX	(read/write)
9	(0x09)	Reserved for TEX	(read/write)
10	(0x0A)	Reserved for TEX	(read/write)
11	(0x0B)	Reserved for TEX	(read/write)
12	(0x0C)	Reserved for TEX	(read/write)
13	(0x0D)	Reserved for TEX	(read/write)
14	(0x0E)	Reserved for TEX	(read/write)
15	(0x0F)	Reserved for TEX	(read/write)

1.9 Gate Array Register List and Definitions

Registers within the TC US's SGAs are accessed using gate array register messages.

No data are passed to the slave in gate array write messages. The register selected for the write implies the data. The gate array access message defines the TCS message fields as follows:

Command Type: Specifies a read or a write
Command Modifier: Specifies which gate array to access

Address Byte: Specifies which register within the gate array to access
Data Byte: Not used.

The decoding of the command type and modifier is as follows:

Command Type 8, Gate Array Read

Command Modifiers:	
0	TC/US SGA #0 Registers
1	TC/US SGA #1 Registers
2	TC/US SGA #2 Registers
3	TC/US SGA #3 Registers
4–15	Illegal Command

Command Type 9, Gate Array Write

Command Modifiers:	
0	TC/US SGA #0 Registers
1	TC/US SGA #1 Registers
2	TC/US SGA #2 Registers
3	TC/US SGA #3 Registers
4–15	Illegal Command

SGA Internal Registers

The Switch Gate Array contains 56 read only registers and 56 write only registers. Each register controls one bit: the address accessed determines the action is taken.

SGA Port Control Registers (Write Only)

Writing these registers with any data enables the drivers or receivers for the indicated ports.

Input Port Controls

0x00 : Enable input port 0
0x01 : Disable input port 0
0x02 : Enable input port 1
0x03 : Disable input port 1
0x04 : Enable input port 2
0x05 : Disable input port 2
0x06 : Enable input port 3
0x07 : Disable input port 3

Output Port Controls

0x08 : Enable output port 0
0x09 : Disable output port 0
0x0A : Enable output port 1
0x0B : Disable output port 1
0x0C : Enable output port 2
0x0D : Disable output port 2
0x0E : Enable output port 3
0x0F : Disable output port 3

SGA Status Registers (Read Only, except SGA Reset Detect FF)

Each of these registers returns one bit in DATA<0> of the return message data field.

SGA Revision Level

0x00 : SGA Revision Number <0>
0x01 : SGA Revision Number <1>
0x02 : SGA Revision Number <2>

SGA Reset Detect Flip Flop (read/write)

0x03 : SGA Reset Detect FF <3> (read/write)
(Always set to zero on power-up)

Input Port Active Bit

0x04 : Input Port 0 Active
0x05 : Input Port 1 Active
0x06 : Input Port 2 Active
0x07 : Input Port 3 Active

Output Port Busy Bit

0x08 : Output Port 0 Busy
0x09 : Output Port 1 Busy
0x0A : Output Port 2 Busy
0x0B : Output Port 3 Busy

Output Port Priority Level

0x0C : Output Port 0 Channel Priority Level
0x0D : Output Port 1 Channel Priority Level
0x0E : Output Port 2 Channel Priority Level
0x0F : Output Port 3 Channel Priority Level

SGA Input Port Signal Assertion Registers (write only)

A write with any data to the following SGA registers asserts the indicated signal. One bit is set at a time: all other bits are unaffected.

Input Port 0	0x34 : Assert input port 0 reverse
Input Port 1	0x35 : Assert input port 1 reverse
Input Port 2	0x36 : Assert input port 2 reverse
Input Port 3	0x37 : Assert input port 3 reverse

SGA Output Port Signal Assertion Registers (write only)

A write with any data to the following SGA registers asserts the indicated signal. One bit is set at a time: all other bits are unaffected.

Output Port 0	0x10 – 0x17 : Assert output port 0, bit<0> – bit<7> 0x30 : Assert output port 0 frame
Output Port 1	0x18 – 0x1F : Assert output port 1, bit<0> – bit<7> 0x31 : Assert output port 1 frame
Output Port 2	0x20 – 0x27 : Assert output port 2, bit<0> – bit<7> 0x32 : Assert output port 1 frame
Output Port 3	0x28 – 0x2F : Assert output port 3, bit<0> – bit<7> 0x33 : Assert output port 3 frame

SGA Input Port Signal Sensing Registers (read only)

The following registers return the indicated bit in DATA<0> of the TCS response message.

Input Port 0	0x10	Read input port 0, bit 0
	0x14	Read input port 0, bit 1
	0x18	Read input port 0, bit 2
	0x1C	Read input port 0, bit 3
	0x20	Read input port 0, bit 4
	0x24	Read input port 0, bit 5
	0x28	Read input port 0, bit 6
	0x2C	Read input port 0, bit 7
	0x30	Read input port 0, frame
Input Port 1	0x11	Read input port 1, bit 0
	0x15	Read input port 1, bit 1
	0x19	Read input port 1, bit 2
	0x1D	Read input port 1, bit 3
	0x21	Read input port 1, bit 4
	0x25	Read input port 1, bit 5
	0x29	Read input port 1, bit 6
	0x2D	Read input port 1, bit 7
	0x31	Read input port 1, frame
Input Port 2	0x12	Read input port 2, bit 0
	0x16	Read input port 2, bit 1
	0x1A	Read input port 2, bit 2
	0x1E	Read input port 2, bit 3
	0x22	Read input port 2, bit 4
	0x26	Read input port 2, bit 5
	0x2A	Read input port 2, bit 6
	0x2E	Read input port 2, bit 7
	0x32	Read input port 2, frame
Input Port 3	0x13	Read input port 3, bit 0
	0x17	Read input port 3, bit 1
	0x1B	Read input port 3, bit 2
	0x1F	Read input port 3, bit 3
	0x23	Read input port 3, bit 4
	0x27	Read input port 3, bit 5
	0x2B	Read input port 3, bit 6
	0x2F	Read input port 3, bit 7
	0x33	Read input port 3, frame

SGA Input Port Signal Sensing Registers (read only)

The following registers return the indicated bit in DATA<0> of the TCS response message.

Output Port 0	0x34	Read output port 0, reverse
Output Port 1	0x35	Read output port 1, reverse
Output Port 2	0x36	Read output port 2, reverse
Output Port 3	0x37	Read output port 3, reverse

SGA Input Port Enable/Disable Sense Register (read only)

The following registers return the indicated bit in DATA<0> of the TCS response message. A one indicates that the port is enabled.

Input Port 0	0x38	Read input port 0 enable/disable sense
Input Port 1	0x39	Read intput port 1 enable/disable sense
Input Port 2	0x3a	Read input port 2 enable/disable sense
Input Port 3	0x3b	Read intput port 3 enable/disable sense

SGA Output Port Enable/Disable Sense Register (read only)

The following registers return the indicated bit in DATA<0> of the TCS response message. A one indicates that the port is enabled.

Output Port 0	0x3c	Read output port 0 enable/disable sense
Output Port 1	0x3d	Read output port 1 enable/disable sense
Output Port 2	0x3e	Read output port 2 enable/disable sense
Output Port 3	0x3f	Read output port 3 enable/disable sense

1.10 Action Register Definitions

Action Register 0, Board Status (read only)

Temp Okay	Spare	Bulk Power OK	Spare	Broad-cast Error	Returns zero	Serial Comm. Error	Slave Proc. Error

Temp Okay
Temperature okay. Indicates that the board's SGA temperature is below the value set in the slaves EEPROM temperature alarm register. Note: The slave turns board power off if the temperature ever exceeds the alarm setpoint. If the slave detects an over temperature state, this register must be read to set "temp okay" back to normal.

Bulk Power OK
Bulk power okay. If this bit is set it indicates that the bulk DC voltage is present and being sensed at the TCUS. A zero indicates that the TCUS is not sensing the bulk DC voltage.

Broadcast Error
Indicates that a broadcast message to this slave has resulted in a negative acknowledgement since the last time the status register was read. This bit is cleared by reading the status register.

Serial Comm. Error
Indicates that a receiver serial communications error was detected by the slave's serial communication hardware since the last read of the status register. This bit is cleared by a read of the status register.

Slave Processor Error
Indicates that the slave processor software entered an illegal state since the last time the status register was read. If this bit is set, either the slave processor must be replaced, or there is a bug in the slave software.

Action Register 1, Control Register (write only)

Spare	Spare	Spare	Spare	Spare	Spare	Spare	Card Reset

Card Reset
Asserting this bit resets the SGAs, clears any gate array execute wires that are asserted, resets the random number generator, and clears the preset on the random number generator. Setting this bit to zero clears the SGA reset wire only.

Action Register 2. Power Control Register (write only)

Spare	Spare	Spare	Spare	Power Margin Level<1>	Power Margin Level<0>	Power Margin Enable	Power On

Power Margin Level<1..0>
Selects the voltage level that the board's power supplies are set to when margining is enabled.

00 = -10%
01 = -5%
10 = +5%
11 = +10%

Power Margin Enable
Sets the board's power supplies to the voltage level selected by the power margin level bits.

Power On
Turns the board power supplies on. Note: The slave only turns power on in response to an individually addressed message; never a broadcast message.

Action Register 3. Previous Message Ack/Nack (read only)

This register always contains the Ack/Nack byte of the previous TCS message. Reading this register clears it.

Spare	Ack Nack Code<5>	Ack Nack Code<4>	Ack Nack Code<3>	Ack Nack Code<2>	Ack Nack Code<1>	Ack Nack Code<0>	Ack Bit

Ack Nack Code<5..0>
This is an acknowledgment code for TCS messages. It is either a positive or negative acknowledgment depending on the sense of the Ack bit in this register.

Nack codes

0 - Null Description
1 - Timeout
2 - Parity Error
3 - Serial Communication Error
4 - Spare
5 - TCS Message Format Error

Ack Codes

0 - Action Register Acknowledge
1 - EEPROM Register Acknowledge
2 - Setup Message Acknowledge
3 - Memory Read Message Acknowledge
4 - Memory Write Message Acknowledge
5 - Gate Array Register Acknowledge
6 - Hardware Register Acknowledge

Ack Bit
This bit indicates that the code is an acknowledgment.

Action Register 4. Clock Check (read only)

A one in this register indicates that low to high transitions were detected on corresponding clock signals.

Each clock checked by this register is monitored for a fixed period of time looking for low to high transitions. The monitoring periods are the following:

Net Time Fan In:	2 msec
Net Time Fan Out:	2 msec
TC/US Hold Time:	2 msec
65 Msec Clock:	160 msec

The total monitoring period is 168 msec. The TCS master will typically time-out reading this action regsiter. The TCS master must take into account the excessive time that the slave takes to respond to this action register.

Spare	Spare	Spare	Spare	Net Time Fan In	Net Time Fan Out	TCUS Hold Time	TCUS 65 msec

Action Register 5. EEPROM Access Enable (write only)

Writing this register with any data enables an EEPROM register write on the next access. This register must be written before each EEPROM write, otherwise a format nack is returned.

Action Register 6. Temperature near SGA #1 and SGA #3 (read only)

This register returns the board's temperature above SGA #1 and SGA #3 at 0.977 °F per tick.

Action Register 7. Clear Execute Wires and RAM Test Register (read/write)

This register has three functions. It is a one byte piece of read/write RAM for testing communication with the TCS Master; anything may be written into it. It clears the gate array execute wires.

Action Register 8. Re-Read Slave Address (write only)

Writing this register with any data instructs the slave to re-read its bay, midplane, and slot number; and to re-initialize its TCS bus address.

Action Register 9. Illegal Register (not applicable)

A read or write of this register returns a format NACK (NACK code 5)

Action Register 10. Illegal Register (not applicable)

A read or write of this register returns a format NACK (NACK code 5).

Action Register 11. Vee Voltage Sensor (read only)

This register returns the voltage detected at the TC/US's -4.5 VDC supply. The value is calculated with the following formula:

Millivolts = (register value)*(36.56 mV per tick) - 6895 mV

Action Register 12. Vtt Voltage Sensor (read only)

This is the bulk Vtt termination power supply voltage sensing register. This register returns the voltage detected at the board's -2 VDC supply. The value is calculated with the following formula:

Millivolts = (register value)*(22.79 mV per tick) - 3333 mV

Action Register 13. LED Control (write only)

This register controls the indicator LED. The LED is initially turned on by a power on reset. Writing the following values to the LED control register results in the called out LED state.

0 - LED off
1 - LED flash at 1 Hz
2 - LED flash at 2 Hz
3 - LED constant on
4-255 - Not Defined

Action Register 14. Illegal Register (not applicable)

A read or write of this register returns a format NACK (NACK code 5).

Action Register 15. Illegal Register (not applicable)

A read or write of this register returns a format NACK (NACK code 5).

Action Register 16. Illegal Register (not applicable)

A read or write of this register returns a format NACK (NACK code 5).

Action Register 17. Temperature near SGA #0 and SGA #2 (read only)

This register returns the temperature above SGA #0 and SGA #2 at 0.977 °F per tick.

Action Register 18. Illegal register (not applicable)

A read or write of this register returns a format NACK (NACK code 5).

Action Register 19. TC/US SGA 0 -3.8 VDC Vee2 Supply Voltage Sensor (read only)
Action Register 20. TC/US SGA 1 -3.8 VDC Vee2 Supply Voltage Sensor (read only)

These registers return the voltage detected at the TC/US's gate arrays' -3.8 VDC supply. The value is calculated with the following formula:

Millivolts = (register value)*(29.23 mV per tick) - 5173 mV

Action Register 21. Illegal Register (not applicable)
Action Register 22. Illegal Register (not applicable)
Action Register 23. Illegal Register (not applicable)
Action Register 24. Illegal Register (not applicable)
Action Register 25. Illegal Register (not applicable)
Action Register 26. Illegal Register (not applicable)

A read or write of these registers returns a format NACK (NACK code 5).

1.11 EEPROM Register Definitions

Slave EEPROM writes take about 20 ms to complete. The Master processor must take into account the long time it takes for the Slave to acknowledge these messages.

The TCS message address byte is the EEPROM register number. The DATA byte is unused in the Read message, and conveys data to be written in the Write message.

All EEPROM registers are read/write.

EEPROM Register 0. Card Type

One byte register allocated for storing the card type. The card type is an ASCII character.

EEPROM Registers 1-16. Board Serial Number

Board serial number registers. This is a block of 16 bytes allocated for storing the BBN board serial number in ASCII format. The least significant character is in register 1.

EEPROM Registers 17 and 18. Artwork Revision Level

Revision level of the printed circuit board part of the board assembly. These registers hold two ASCII characters that represent the revision level of the circuit card. The least significant character is in register 17.

EEPROM Registers 19 and 20. Electrical Revision Level

The revision level of the circuitry of the circuit board. This is used to keep track of the implementation of Engineering Change Orders (ECOs) on the circuit card. These registers hold two ASCII characters that represent the electrical revision level of the circuit card. The least significant character is in register 19.

EEPROM Registers 21 and 22. Slave Software Revision Level

Revision level of the firmware in the 68HC11. This is a two character alphanumeric value. The least significant character is in register 21.

EEPROM Register 23. Temperature Alarm Setpoint

This register contains the analog to digital converter reading at which the slave considers the board too hot. At this value the slave shuts off board power and flags temperature error in the board status register. The units of this register are the same as for the temperature sensor action register: 0.977 degrees Fahrenheit per tick.

EEPROM Register 24. A/D Converter TCS Vcc Nominal Reading

This register stores the analog to digital converter reading that results when TCS Vcc power supply is at 5.00 VDC. This register is pro-

grammed at the factory, and is referenced by the TCS master processor when reading the TCS Vcc voltage sensing register to calibrate the results for analog component tolerances. The register's units are the same as those of the Vcc voltage sensing action register, 24.4 mV per tick.

EEPROM Register 25. Vee A/D Converter Nominal Reading

This register stores the analog to digital converter reading that results when Vee power supply is at -4.5 VDC.

EEPROM Register 26. A/D Converter Vtt Nominal Reading

This register stores the analog to digital converter reading that results when Vtt power supply is at -2 VDC.

EEPROM Register 27. A/D Converter SGA 0 Vee2 Nominal Reading
EEPROM Register 28. A/D Converter SGA 1 Vee2 Nominal Reading

Millivolts = (register value)*(20.5 mV per tick) - 2750 mV

These registers store the analog to digital converter reading that results when the indicated gate array's Vee2 power supply is at -3.8 VDC.

EEPROM Register 29. Reserved for TEX
EEPROM Register 30. Reserved for TEX

EEPROM Register 31. Board Group ID

Stores the board's broadcast group identifier. When the slave receives a broadcast message it compares the LS_SLOT_ID to this register to determine whether the message is meant for this board's broadcast group.

1.12 Hardware Register Definitions

The hardware registers are the raw board registers the slave controls. All hardware registers are either write only or read only. Note: Many of the bits in the TC/US hardware write registers manipulate low level device control signals that are meant to be altered only by the slave.

TCS messages select between hardware registers with the command modifier field of the command byte.

The address byte is unused.

The data byte specifies any write data.

Write Register 0. Net Time Select. Random Number Generator Control (write only)

Margin Control B	Margin Control A	Monitor Control <0>	Monitor Control <1>	Monitor Control <2>	Monitor Control <3>	Monitor Control <4>	LED Control

Margin Control <B..A>
These bits control the level at which the voltage is margined when voltage margining is enabled.

Monitor Control <0..4>
These bits control the selection of the function that will be monitored. Monitor Control <0..1> select the temperature or voltage that is converted by the A/D while Monitor Control <2..4> select digital signals that are monitored.

LED Control
This bit turns the LED on and off.

Write Register 1. TCS Bus Enable <8..9>. Margin Control. Power Control (write only)

TCS from Slot 8	TCS from Slot 9	Voltage Margin Disable	Power Enable	Spare	Spare	Spare	Spare

TCS Bus Enable <8..9>
These bits enable the TCS bus from each of the other two possible switch cards. The TC/US cards in the Server and Requester slots must be enabled at the TC/US in order for the master to hear those slaves' respones.

Voltage Margin Disable
Clearing this bit connects voltage trimming resistors to the trimming circuitry for the board's power supply via an analog multiplexor. The multiplexor channel is selected with two bits controlled by the TC/U S's Hardware Register 0.

Power Enable
Turns on the board's power supply.

Write Register 2, TCS Bus Enable <7..0>

This register enables the TCS bus from each of 7 function cards. Writing a one gates a function card's slave to master bus driver onto the TCS bus. The function card must be enabled at the TC/US in order for the master to hear those slaves' responses.

TCS from Slot 7	TCS from Slot 6	TCS from Slot 5	TCS from Slot 4	TCS from Slot 3	TCS from Slot 2	TCS from Slot 1	TCS from Slot 0

Write Register 3, SGA Reset, Random Reset, Random Preset, Gate Array Execute

SGA Reset	Random Number Reset	Random Number Preset	Spare	TC US SGA 3 Execute	TC US SGA 2 Execute	TC US SGA 1 Execute	TC US SGA 0 Execute

SGA Reset
Asserting this bit holds the four SGAs on the TC/U S reset. Clearing this bit releases the reset.

Random Number Reset
Holds the board's random number generator reset at zero. (The random number is used by the SGAs to arbitrate between equal priority switch messages.)

Random Number Preset
Holds the board's random number generator at one.

SGA Execute <3..0>
These bits control the assertion of the gate array execute signals. The execute signals are part of the TCS slave to gate array interface circuitry. The execute signals are manipulated by the slave in conjunction with its serial peripheral interface. The master should never need to modify this register. It is controlled by other register accesses.

Write Register 4, Net Time Enable <7..0>

Net Time <7>	Net Time <6>	Net Time <5>	Net Time <4>	Net Time <3>	Net Time <2>	Net Time <1>	Net Time <0>

Net Time Enable <7..0>
Selects which of the eight function cards' net time signals passes up to the TC/CLK.

1.12.1 Read Register Definitions

Read Register 0 (read only)

No Connect	No Connect	No Connect	No Connect	Status <2>	Status <1>	Status <0>	Bay ID<2>

No Connect
Undefined.

Status <2..0>
Status<2> monitors the state of the Margin Disable signal from Hardware Register 1. Status<1> monitors the state of the Power Enable signal from Hardware Register 1, and Status<0> monitors the state of the +/- 24VDC power supply.

Bay ID<2>
This is the most significant bit of the 3 bit bay number for this slave. This bit is read off of the midplane where it is set with DIP switches.

Read Register 1 (read only)

No Connect	No Connect	No Connect	No Connect	Bay ID<1>	Bay ID<0>	Mid-plane ID<2>	Mid-plane ID<1>

No Connect
Undefined.

Bay ID<1..0>
These are the two least significant bits of the 3 bit bay number for this slave. These bits are read off of the midplane where they are set with DIP switches.

Midplane ID<2..1>
These are the two most significant bits of the three bit midplane number. This bit is read off of the midplane where it is set with DIP switches.

Read Register 2 (read only)

No Connect	No Connect	No Connect	No Connect	Mid-plane ID<0>	Slot ID <2>	Slot ID<1>	Slot ID <0>

Midplane ID<0>
This is the least significant bit of the three bit midplane number. This bit is read off of the midplane where it is set with DIP switches.

Slot ID <2..1>
These are the three bits of the three bit midplane number. These bits are read off of the midplane where they are set with DIP switches.

Slot ID <0> (aka A or B* Switch Card)
This bit indicates which of the two possible sets of switch cards (i.e. A or B) in a midplane this card belongs to.

Read Register 3 (read only)

No Connect	No Connect	No Connect	No Connect	Card Type<3>	Card Type<2>	Card Type<1>	Card Type<0>

Card Type <3..0>
This is the board card type that is read off the midplane.