•plevin

doc126

*** Request Q00000.19103 for plevin@cheese.bbn.com Mon Aug 15 11:49:33 1988

Account:	2128022
Submitted.	Mon Aug 15 11:50:48 1988
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FILE: doc_26
DATE: 06-26-88
PURPOSE: Discusses the findings of the final layout for the SIGA.

GENERAL

This is the results of MOSTLY static analysis of the SIGA with the final SEGLEN file.

CRITICAL TIMING (from doc_19)

- All clock-to-q requirements (SIGA.SCL1A)
  Re-ran the simulation under /usr/plevin/siga/design/siga/sim
  Clock-to-q timing looks better than estimated (.BLOCKS)

- All requirements addressed by the lcap_siga.XX files.
  All look good and indicate that both Switch interfaces could run at 45 Mhz under wccom.

- Core to output register hold-time for T_CLK

  From SIGA.BCRFLST (bccom):

  b/c to "core" = 1.35 (to postdriver B)
  1.01* (b/c postdriver delay)

  2.36 ns

  *actually, there was one segment faster, at 0.94 ns. This was: U_RQ_BI/CT/USTE_WRITE3/U0. But the data path skew was ~ 5ns, so this path was eliminated.

  ...since,

  w/c UT_CLK seg = 2.39 ns

  ...then hold-time margin BEFORE any data path skew is:

  2.36 - 2.39 = -0.03 ns

  Of course, there is no matching involved here, this is EXTREMELY worst-case.

  The fastest data path (after bogus paths were elimated) was found by lcap_siga.6a to be: 1.8 ns (after setup subtraction). So:

  1.8 - .2 (hold-time of a F/F @bccom) = 1.6 ns

  and so margin is:

  -0.03 + 1.6 = 1.57 ns, which is plenty

- T_ENA_HOLD worst-case skew

@ wccom: 4.34/4 15 (U_TI_CT_MIN_LAT_AD[illegible]G) which is about the best that I can hope for.

- TBUS Input latches setup/hold time
  Given the T_ENA_HOLD timing, I think that I can create an external signal that will make the setup/hold time work.

- TIU sneak path relative to T_CLK

  These are the lcap results:

	BC Data Path	WC Clock Path	
@ wccom:	11.1/10.9	5.55/5.46	(U_TI_DA/UPAD_OUT_TDAT.22(CP))
@ nom:	6.3/6.2	3.58/3.53	(U_TI_DA/UPAD_OUT_TDAT.22(CP))
@ bccom:	3.6/3.5	2.39/2.37	(U_TI_DA/UPAD_OUT_TDAT.22(CP))

  But because of the limitations in lcap (mentioned in lcap_siga.2), the real margin at bccom is:

```
  3.50
-  .70 (lcap added-in setup)
-  .20 (lcap excluded hold)
- 2.39 (w/c clock)
======
   .21 ns margin
```

  Although this does not seem like much, there are two things to consider: First, I have not matched paths, I have simply taken the "worst and the worst." Second, this margin is about 8%, relative to T_CLK. In addition, this all is assuming 0 ns hold time on the Fast input pins to the SIGA. In reality, the hold-time is specified by the T-Bus spec at 2 ns. Even 1 ns would probably do as sufficient margin for this path.

- Hold at the Parity Error latch on the TCU and Server

- Skew between T_CLK and F_CLK elements

  Worst-cast UF_CLK @ wccom is: 0.45 ns. This is certainly better than any possible T_CLK segment. So, this is fine.

- Skew between intercommunicating elements on T_CLK

  One of the worst things here is the skew between the USH_TDATxxx, USH_TRANSxxx in the TI_CT and the output registers in TI_DA. Typically the output registers' clock is lagging the control registers. This is not good since the control register feeds the output register. However, using lcap_siga.6b, we see that the fastest possible data path in ANY of the TI_CT and TI_DA is: 1.8 ns (without lcap setup).

  The clock skew between the fastest register in TI_CT and TI_DA is: 2.39 - 1.33 = 1.06. So that at absoulte worst-case, the hold margin is:

```
  1.8
- 1.06
-  .2  (hold-time of F/F @ bccom)
  ====
   .54 ns
```

This is not a bad number since the hold time margin in a shift-register configuration with no clock skew is:

```
    .7  (min prop dly of FD1P @ bccom)
-   .2  (min hold-time requirement of FD1P @ bccom)
===
 .5 ns
```

However, I decided to grind through some matching to get a better picture of the actual hold-time. The file: lcap_siga.special shows this analysis. It is a page taken from the file: SIGA.BCRFLST.It turns out that the worst offender in terms of hold-time are the enable flops for the output tri-state drivers located in TI_DA. These have a short data path and a long clock skew.

Even so, considering that the earliest F/F in TI_CT feeding anything in TI_DA can be clocked at 1.33, looking at the lcap_siga.special file, it is seen that the sneak data paths are always AT LEAST AS LARGE as the absolute clock skew at the flip-flop. (I only calculated the sneak path for those clock skews over 1.6 ns). Therefore, the true margin is at least:

```
  1.33
-  .2  (hold-time @ bccom)
  ====
~ 1.0     This should be sufficient.
```

The clock skew within the TI_CT is pretty small (1.9 - 1.33 = .57) and I don't see any problems there

- FQ_Valid delay

- Worst-case skew between the T,R,S _CLK's and repeated core clock
  Done in lcap_siga.5

- T-Bus hold requirements for write to Rams (affects T_ENA_HOLD requirements)

  The w/c scenario is for the data which must be clocked in a ripple fashion into RAM1's,latches and other F/F's. It is very difficult to follow all of the paths manually so I came up with what I beleive to be a good "guesstimate" at the actual w/c ripple path delay for the Requstor and Server.

  For the Requestor and Server:(@wccom)

```
 4.39  w/c T_CLK to postdrivers
 3.28  w/c postdrivers
 7.00  w/c guesstimated clk-to-q of internal F/F to ram,latch,F/F
 0.80  typical hold-time of ram,latch or F/F
-0.80  allowance for b/c sneak clock path
=====
14.7   min hold-time requirement for data
```

  This is, of course, pessimistic for two reasons: 1) no matching was done and 2) I did not include the minimum delay on the data path which has to go through an input buffer and an input latch. Nor did I add in the sneak delay of the T_ENA_HOLD path through the input latches.

- R_DATA, S_DATA, R_REVERSE, S_FRAME, M_SIXTY_FIVE setup and hold requirements.

Requestor data/reverse setup: (@wccom)

```
 1.36  w/c data path to data and reverse F/F's
 1.50  F/F setup requirement
-1.50  allowance for sneak clock path
=====
 1.36  min setup
```

Requestor data/reverse hold: (@wccom)

```
 2.89  R_CLK to postdrivers
 2.61  w/c postdrivers to data and reverse F/F's
 0.74  hold-time of a F/F @wccom
-0.74  allowance for sneak data path @wccom
=====
 5.50  min hold
```

Sixty_five setup: (@wccom)

```
 1.54  w/c data path to U_RQ_TM/RP/U14(D)
 1.50  F/F setup requirement
-1.50  allowance for sneak path clock
=====
 1.54  min setup
```

Sixty_five hold: (@wccom)

```
 2.89  R_CLK to postdrivers
 2.32  w/c postdrivers to sixty_five F/F (RQ_TM/RP/U14(CP))
 0.74  hold-time of a F/F @wccom
-0.74  allowance for sneak data path @wccom
=====
 5.21  min hold
```

Server data/frame setup: (@wccom)

```
 1.75  w/c data path to data and frame F/F's
 1.50  F/F setup requirement
-1.50  allowance for sneak clock path
=====
 1.75  min setup
```

Server data/frame hold: (@wccom)

```
 2.89  R_CLK to postdrivers
 2.47  w/c postdrivers to data and frame F/F's
 0.74  hold-time of a F/F @wccom
-0.74  allowance for sneak data path @wccom
=====
 5.36  min hold
```

- R_CLK, S_CLK duty cycle requirements

The constraints on the duty cycle are as follows:

1) Duty cycles' affect on the setup/hold at the SIGA via the LCON. This because the LCON clocks out on the negative edge and the SIGA clocks in on the positive edge.

2) There must be enough internal hold time (high [RS]_CLK) for the

internal register to latch data into the RAM1 cells relative to the positive edge of [RS]_CLK.

3) Minimum pulse width of internal F/F's and latches.

It is unlikely that the limit for #3 above will ever be reached. So I focused on #1 and #2. First, looking at constraint #1, the LCON claims to give a setup/hold to the SIGA of 7.8/14.2 at exactly a 50% duty cycle. Therefore, INCREASING the high time of [RS]_CLK reduces the setup and REDUCING the low time reduces the hold.

Using constraint #1:

The MAXIMUM high time is:

```
 12.50  [RS]_CLK high time at 50% duty cycle
  7.80  setup at SIGA from LCON with 50% duty cycle
 -1.75  w/c data/frame/reverse setup requirement at SIGA
  ====
 18.5   MAXIMUM allowable HIGH time for [RS]_CLK
```

The MINIMUM high time is:

```
 12.50  [RS]_CLK at 50% duty cycle
-14.20  hold at SIGA from LCON with 50% duty cycle
  5.50  w/c data/frame/reverse hold requirement at SIGA
  ====
  3.8   MINIMUM allowable HIGH time for [RS]_CLK
```

Using constraint #2:

The MINIMUM high time is:

```
 12.50  [RS]_CLK at 50% duty cycle
-14.20  hold at SIGA from LCON with 50% duty cycle
  7.00  w/c delay from internal [RS]_CLK to latch or F/F
  ====
  5.3   MINIMUM allowable HIGH time for [RS]_CLK
```

Therefore, the maximum allowable range of HIGH [RS]_CLK, assuming a 25 ns clock period is:

[RS]_CLK range = 5.3 to 18.5 ns

- General hold-times in all modules

Requestor Switch modules

The maximum clock skew on the core Requestor Switch clock is 0.37 ns.

UR_CLK has the postdirvers on the farthest delay of the net so there are not hold-time problems between the Requester core and the output registers.

Using lcap_siga.7 everything looks O.K.

***End of request Q00000.19103 for plevin@cheese.bbn.com Mon Aug 15 11:49:40 1988

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Printed on queue freshqms, device freshqms
5 pages of output
1 file printed
Used 600 milliseconds of runtime

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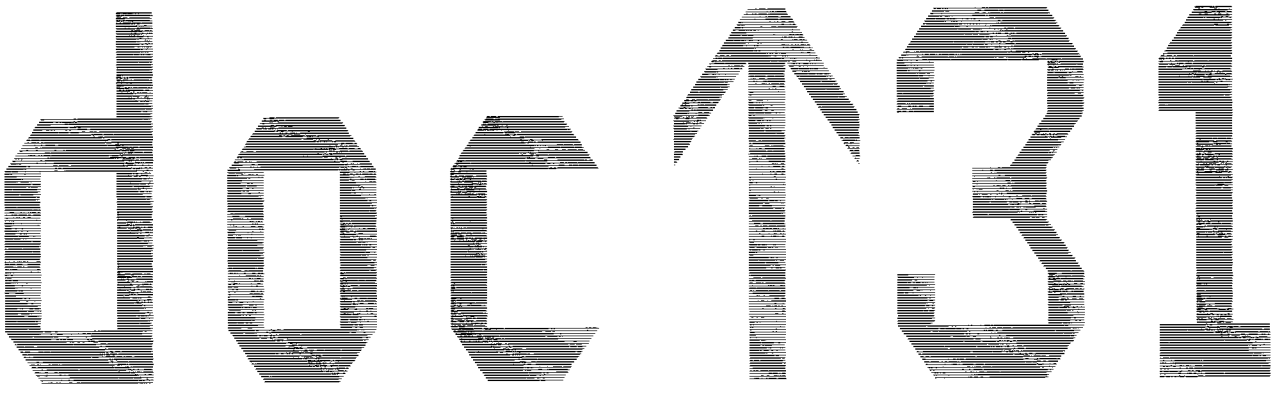

*** Request Q00000.19104 for plevin@cheese.bbn.com Mon Aug 15 11:50:17 1988

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FILE: doc_31 SIGA (DESIGN) SIGA LOGIC DESCRIPTION
CREATED: July 26, 1988
PURPOSE: To document the design of the SIGA

INTRODUCTION:

This document, in addition to the attached documents and drawings, will provide a guide for understanding the SIGA design by "walking through" the hierarchies of the schematics.

It is assumed that the reader has read and is familiar with the SIGA Functional Specification - by Philip Levin. That specification should be used in conjunction with reading this specification.

HEIRARCHY NAMING CONVENTION:

The standard naming convention used in the schematics is now described...

Standard abbreviations:

TOP LEVEL:

RQ Requestor
SV Server
CS Configuration/Status Unit
TC Test and Control Unit
TI TBus Interface Unit

SECOND LEVEL:

BI Bus Interface Unit
ST Switch Transmit Unit
SR Switch Recieve Unit
IO Switch I/O Unit
CN Configuration Unit
TM Switch Timers/Counters (used only by the Requestor)
CM Command Module (used only by TCU)

RG Registers (used only by TCU)

THIRD LEVEL:

CT Controller (i.e. FSM)
DA General Data path logic (usually associated with FSM)

Other abbreviations:

GENERAL:

Dd..d where d..d is a string of no more than 7 characters. This applies to any part which is a DeMorgan's equivalent.

Xd..d where d..d is a string of no more than 7 characters. This applies to any part for which you do not want to have a hierarchical name and are not already DeMorgan's equivalents, such as parts common to many hierarchies.

It also applies to any element that is more then three levels deep.

A list of all hierarchies and a brief definition follows...

Hierarchy Name	function (if not implied by naming convention)
TC_RG_CD	COMMAND DECODER
TC_BI	TCU BUS INTERFACE
TC_RG	TCU REGISTERS
TC_RG_IO	IO CELL FOR TBUS RESPONSES
TC_RG_DR	TCU DATA REGISTERS (RAM1'S)
TC_RG_DL	TCU DATA REGISTERS (LD2P'S)
XCNTA	COUNTER BIT - UP,CLEAR,LOAD
XCNTC	COUNTER BIT - DOWN,CLEAR
XCNTD	COUNTER BIT - JOHNSON,LOAD
XCNTE	COUNTER BIT - DOWN, LOAD
XCNTF	COUNTER BIT - DOWN, LOAD
XCNTG	COUNTER BIT - DOWN, LOAD
XCOUNTA	COUNTER - 4-UP USING XCNTA
XCOUNTD	COUNTER - 4-JOHNSON USING XCNTD
XCOUNTE	COUNTER - 4-DOWN USING XCNTE
XCOUNTG	COUNTER - 4-DOWN USING XCNTG
CS_CT	CSU CONTROLLER
CS_DA	CSU DATA MODULE
XDM12L	1-TO-2 DECODER, DUAL ENABLE, LOW-TRUE OUTPUT
DAN2	DEMORGAN 2-IN AND GATE
DAN4	DEMORGAN 4-IN AND GATE
XDEC2T4H	2-TO-4 DECODER, UNCOMPLEMENTED OUTPUT
DND2	DEMORGAN 2-IN NAND GATE
DND3	DEMORGAN 3-IN NAND GATE
DND4	DEMORGAN 4-IN NAND GATE
DND6	DEMORGAN 6-IN NAND GATE
DNR2	DEMORGAN 2-IN NOR GATE
DOR2	DEMORGAN 2-IN OR GATE
XFDPAN	STATE MACHINE BIT
XREQ_GEN	SERVER REQUEST GENERATOR
RQ_BI	REQUESTOR BUS INTERFACE MODULE
RQ_BI_CT	REQUESTOR BUS INTERFACE CONTROLLER
RQ_BI_ER	REQUESTOR BUS INTERFACE ERROR HANDLER
RQ_BI_RS	REQUESTOR BUS INTERFACE TBUS RESPONSE GENERATOR
RQ_BI_TI	REQUESTOR BUS INTERFACE TBUS R/W INTERFACE
XPRA_GEN	RAND # GEN FOR PHYSICAL ROUTE ADDR
RQ_TM	REQUESTOR TIMER MODULE
RQ_TM_CO	REQUESTOR CONNECTION TIMER
RQ_TM_PT	REQUESTOR PRIORITY TIME SLOT LOGIC
RQ_TM_RJ	REQUESTOR REJECT LOGIC
XREJ_TIM	REQUESTOR REJECT TIMER
RQ_TM_RR	REQUESTOR RANDOM START/RETRY MODULE
XRSR_BOC	REQUESTOR RANDOM START/RETRY BACKOFF COUNTER
XRSR_MSK	REQUESTOR RANDOM START/RETRY MASK LOGIC
XRSR_RND	REQUESTOR RANDOM START/RETRY RANDOM NUM GEN
RQ_TM_RC	REQUESTOR REAL TIME CLOCK
RQ_TM_RP	REQUESTOR REAL TIME PRESCALER
RQ_TM_SU	REQUESTOR SYNCHRONOUS ACCESS UNIT
RQ_TM_SR	REQUESTOR SLOTTED START/RETRY MODULE
RQ_TM_TS	REQUESTOR TONI SUBTRACTION LOGIC
XTONI_SB	REQUESTOR TONI SUBTRACTOR

RQ_CN	REQUESTOR CONFIGURATION MODULE
RQ_IO	REQUESTOR I/O REGISTER MODULE
RQ_SR	REQUESTOR SWITCH RECEIVER MODULE
RQ_SR_CT	REQUESTOR SWITCH RECEIVER CONTROLLER
RQ_SR_DA	REQUESTOR SWITCH RECEIVER DATA
RQ_ST	REQUESTOR SWITCH TRANSMITTER MODULE
RQ_ST_CT	REQUESTOR SWITCH TRANSMITTER CONTROLLER
RQ_ST_DA	REQUESTOR SWITCH TRANSMITTER DATA
XTX_REGF	REQUESTOR SWITCH TRANSMITTER TRANSMIT REGISTER FILE
XRSP_DEC	SERVER RESPONSE DECODER
XRSP_GEN	SERVER RESPONSE GENERATOR
SV	SERVER MODULE
SV_CN	SERVER CONFIGURATION MODULE
SV_IO	SERVER DATA I/O MODULE
SV_BI	SERVER BUS INTERFACE
SV_BI_CT	SERVER BUS INTERFACE CONTROLLER
SV_SR	SERVER SWITCH RECEIVER
SV_SR_DA	SERVER SWITCH RECEIVER DATA
SV_SR_CT	SERVER SWITCH RECEIVER CONTROLLER
SV_ST	SERVER SWITCH TRANSMITTER MODULE
SV_ST_DA	SERVER SWITCH TRANSMITTER DATA
SV_ST_CT	SERVER SWITCH TRANSMITTER CONTROLLER
XTX_SRLZ	SERVER STORAGE/SERIALIZER
XTX_WORD	SERVER TRANSMIT WORD LOGIC
XSR_LAT	SERVER SET/RESET LATCH
XSTRT_TB	SERVER START TBUS
XSYNC	SERVER/REQUESTOR VARIABLE-DELAY SYNCHRONIZER
XSYNC_FX	SERVER/REQUESTOR FIXED-DELAY SYNCHRONIZER
TI_CT	TIU CONTROLLER
TI_CT_DT	TIU ADDRESS DETECTOR
TI_CT_SH	TIU SAMPLE AND HOLD
TI_DA	TIU DATA REGISTER
X	NET EXPANDER

Below is the hierarchical list of the SIGA components...

```
SIGA

   CS_DA
      XLD1X32
      X

   TC_BI
      XRSP_DEC
         DND6
         DOR2
         DND3
      DND2
      DNR2
      XSYNC_FX
      DND3
      XFDPAN
      DND4

   SV_BI
      SV_BI_CT
         XST_TBUS
            DND3
         DND3
```

```
        DNR2
        DOR2
        XFDPAN
        DND2
    XREQ_GEN
    XSYNC
    XRSP_DEC
        DND6
        DOR2
        DND3
    XRSP_GEN
        DNR2
        DND2
        DND4
        XSR_LAT

TC_RG
    TC_RG_DL
    TC_RG_CD
    XDEC2T4H
    TC_RG_IO
    TC_RG_DR

RQ_CN
    X
    XLD1X32

RQ_ST
    RQ_ST_CT
        XFDSC
        X
        XSYNC
        XFDSA
        XFDPAN
    RQ_ST_DA
        XTX_REGF
        XFDSA
        XFDSB
        XFDSC
    XSYNC_FX

RQ_BI
    RQ_BI_RS
        X
    RQ_BI_ER
        XFDSA
    RQ_BI_TI
        XPRA_GEN
        XFDSA
        X
    RQ_BI_CT
        XFDSC
        XSYNC
        XFDSA
        XFDPAN

RQ_SR
    RQ_SR_DA
        XFDSC
        XFDSA
```

```
      XFDSB

   RQ_SR_CT
      XFDSC
      XFDSA
      XFDPAN

   XSYNC_FX

RQ_IO
   XFDSC

RQ_TM
   RQ_TM_SU
      XFDSB
      XFDSA
   RQ_TM_PT
      XFDSA
   RQ_TM_RR
      XRSR_RND
      XRSR_BOC
         XCOUNTE
            XCNTE
      XFDSA
         XCOUNTD
            XCNTD
      XRSR_MSK
   RQ_TM_RP
      XCNTC
         XFDSB
   RQ_TM_RJ
      XFDSC
      XREJ_TM
         XCNTF
   RQ_TM_CO
      XFDSC
      XCOUNTG
         XCNTG
   RQ_TM_TS
      XTONI_SB
   RQ_TM_RC
      XCOUNTA
         XCNTA
            XFDSB
   RQ_TM_SR
   XSYNC_FX

CS_CT
   XFDSA
   XFDSB
   XFDPAN
   XSYNC_FX

TI_CT
   TI_CT_SH
   TI_CT_DT
   X

TI_DA
SV_IO
```

```
SV_ST
   SV_ST_CT
      DOR2
      XTX_WORD
         DOR2
         XDM12L
      DND4
      DND3
      DAN2
      DND2
      DNR2
   SV_ST_DA
      XTX_SRLZ


SV_SR
   SV_SR_DA
      DAN2
      DNR2
      DAN4
      DND2

   SV_SR_CT
      DND6
      DND4
      DND3
      XFDPAN
      DND2
      DNR2

   XSYNC
   XSYNC_FX
   DOR2
   DND2
   X

SV_CN
   X
```

Below begins the walkthrough of the various IMPORTANT hierarchies.

NOTES:

1) All page reference numbers refer to the SIGA schematics.

2) Most negated signals in the schematic are are preceded by an "N". A single exception to this rule is "NXT_xxxx," which is generally used to indicate "next" in a signal name. "Next" indicates that the signal "xxxx" will be valid after the next clock transition. When the form "NXT_xxxx" is to be negated, it is indicated by "NNXT_xxxx."

3) For all state diagrams, the numbers next to branches correspond to the signal on the schematic. In addition, all states in the state diagram correspond to states in the schematic for that controller. For example, in the CSU, "NSTE_IDLE_BR1" corresponds to "State Idle - Branch #1."

4) All state machines are designed around the "state per bit" concept. There

is no encoded states. This increases the number of state bits, but decreases the number of terms per state and removes the need for sate decoding. It also makes it easier to follow the schematic.

5) Most handshaking (especially across synchronizers) is done as "differential" rather than "full" handshaking. With differential H/S, when the master wants to initiate an operation, it loads its EXECUTE handshake with the opposite state of the slave's COMPLETED handshake. The slave, seeing the difference, interpretes this as a GO. When the Slave is complete, it loads the value of the master's EXECUTE into its COMPLETED and the master recognizes this as a DONE. Note that with this method, there is no way to "interrupt" a pending operation. This is why the Server has to use an additional handshake pair to implement the interrupt function.

6) Sometimes a state of a State Machine will be represented as "FAST_STE_xxxx" instead of just "STE_xxxx." This is a "faster" version of the particular state in that it is created directly from the state bit and not from the FB output of the FDPAN.

7) In the module descriptions, a "*" is used as a wildcard for signal name descriptions.

SIGA: There are 17 top-level hierarchies that comprise the entire SIGA. Each hierarchy MAY have other sub-hierarchies below it. Those sub-hierarchies are described below. The SIGA module also contains all of the pad buffers and the nand-tree chain connections.

CS_DA: Check for illegal CSU access. Create the CSU_CTL bus which contains all the write enables and write mask. Contains the Interleaver_Address Register.

TC_BI: T-Bus interface for the TCU. Contains state machine and input latches for the T-Bus. UXSYNC_FX takes the execute command from the TC_RG_CD. This occurs when a read of register address 8 is performed from the TCU interface. The state machine is a stripped-down version of the Server T-Bus master state machine - i.e., it does not support non-byte-transfers or become an observing master.

XRSP_DEC: Used in T-Bus controllers to decode responses from the T-Bus. This also generates the HOLD_OK signal. This is used to freeze the Server state machine for things like slave-pause, Promise, etc.

XSYNC_FX: Fixed-delay synchronizer. This module has a delay of 9 -17 clock ticks, depending on when the input is present relative to the 3-bit ripple counter. This is used in various applications where the actual delay does not matter. Note that input to this module must be stable for at least 17 clock ticks. It is used for level-type handshakes. The NASYNC_CLR input is used for special and separate reseting. This signal is created by making M_NRESET and M_NDEBUG low at the same time. This is just a hack for simulation purposes. In normal operation, this is NOT necessary.

XFDPAN: State machine bit. The reset for the state machine is not directly anded to the D-input because this would affect set-up time. Instead, any branching equations (which always require current state info) are derived from the FB output. When all the NRES pins of a particular state machine are asserted (=0), all "current state" bits in branch equations go to "0." In this manner, all states get reset. In fact, the

only state which must be treated differently is the reset (usually IDLE) state. This state bit must have its NRES pin tied high. Then the global state machine reset must be a term on the D-input to the IDLE state bit equation. This technique can be seen in any state machine in the Requestor.

SV_BI: Bus interface for the Server. Handles data to/from the T-Bus for the Server. It is activated by some event on the Switch interface such as a new message or a loss of Frame. The Server uses two handshakes in each direction - XFER_REQ/TERM_REQ from the Switch interface - and sends back XFER_COMP/TERM_COMP to the Bus interface. The XFER_REQ/XFER_COMP signals are analogous the Requestor's EXEC and COMPLETED. They are differential handshakes. The TERM_REQ-TERM_COMP are used to "interrupt" pending operation without creating a race condition. This is used during drop-lock operations.

SV_BI_CT: Controller for the Server T-Bus interface. STATE_A is the Address phase of a T-Bus access. STATE_I is the idle state. STATE_DATA[0..3] is one of four data states used for reads or writes.

XST_TBUS: Starts the T-Bus transaction by generating the T-Bus request. Also controls when the T-Bus is driven.

XREQ_GEN: Loads the correct value into the T-Bus transaction fields.

XSYNC: Variable-delay synchronizer. Should never be re-configured during normal operation. U20, U0, U19 comprise the phase generator. U1 selects the correct phase. U2 and U22 select which clock edge is active. U16,U17,U18 feed the output of the phase generator into the capture F/F's (U5-U10). U15 selects the desired (settled) output. The NRES input is used for special and separate reseting. This signal is created by making M_NRESET and M_NDEBUG low at the same time. This is just a hack for simulation purposes. In normal operation, this is NOT necessary.

XRSP_GEN: Generate the Switch message response from the T-Bus response. Generate the prioritized error codes, if any. Otherwise, detect and pass any T-Bus slave error codes.

TC_RG: Contains the storage modules for all T-Bus transactions (both directions). U14 serializes all bits from a given register for reading-out on the TCU serial port.

TC_RG_DL: Same as a TC_RG_DR except that it is set to all 1's upon power-up reset. This gives the CSU_Map value a default setting of all 1's.

TC_RG_CD: Shifts-in the TCU serial input. Counts the bit address for reading data out of the TCU. NEXEC (from C_NEXECUTE), when high (=1), allows the shift registers, U35.* and U32.*, to load and hold data. This also clears the bit counter.

TC_RG_IO: Storage module that allows 2-way storage. In one direction, it puts data which was loaded serially via the TCU port, onto the T-Bus. When the T-Bus responds, it latches-in the Response data from that same field.

TC_RG_DR: This is the unidirectional version of TC_RG_IO. It is used for placing data on the T-Bus with no requirement for returned data.

RQ_CN: Configuration module for the Requestor. Contains configuration registers and TONI registers.

X: This is a hack to get around limitations of the schematic entry software. It is used to break-out a bus.

RQ_ST: Requestor Switch Transmitter controller and data modules. Handles all Switch transmit functions.

RQ_ST_CT: Implements the STU state machine. STU_ERRORS are created by recording the branch that the state machine takes to get to DONE or LOCKED-DONE. Rej_Abort and Rej_Timeout are prioritized. Rejects or message responses are latched while the STU is transmitting and are recognized by the STU during WAIT.

COUNT_DONE indicates that whatever Switch START/RETRY mechanism has been chosen, the STU is free to continue. The CLEAR state is used for the following reason: If the STU has a CONN_TO (Connection timeout) while in wait, it should immediately transition to DONE, then IDLE. In IDLE, the STU is ready to take a new Function Request. However, the SRU may just be receiving a four-word read message and not ready to go back to its IDLE state. The SRU must be in its IDLE state by the time the STU commands a new transaction, otherwise the SRU will not get "armed." Therefore the CLEAR state of the STU is inserted to allow time (16 Switch clock ticks) for the SRU to complete any possible incoming message.

The SRU gets "armed" whenever the STU enters BID1 or CMD. The lower-half of each state machine bit represents the state of Frame.

RQ_ST_DA: Calculates the checksum, handles priority promotion, assembles message components, contains storage modules for the transmitted words. The checksum calculation is especially slow which is why it is split to both sides of the pipeline.

XTX_REGF: Transmit register file. U8 ensures that when the module is not being selected, RAM1_1 is enabled so that the bus into U0 is never floating.

RQ_BI: The Requestor Bus Interface. This module contains the sub-modules necessary to interface the Requestor with the T-Bus. Whereas most top-level modules contain a _CT (controller) and _DA data portion, the RQ_BI has a controller portion (RQ_CT), but the data portion is split-up among the RQ_RS, RQ_BI, and RQ_ER modules.

RQ_BI_RS: Handle all Requestor responses to the T-Bus. Note that responses during [LOCKED] IDLE are handled in the TIU. This was done to move this time-critical logic closer to its inputs (the TIU - which has a specific placement during layout). Of interest is the fact that during BREQ, the locked Requestor will always respond with REFUSED-LOCKED, even to its locked Master. The Requestor does not check (U22) for this unusual condition. This is an optimization to reduce critical timing in the Requestor. The 3-to-1 muxes, U70.* put the appropriate error code on the T-Bus if an error occurs.

RQ_BI_ER: The error module collects Switch and Remote Errors, generates and collects Function Request Errors (FQ_Errors), prioritizes the errors and encodes them. NFIRST_LOCKED is true (=0) when the Requestor BIU has just been OPENED. This event also causes LOCKED to be asserted (the Requestor is considered locked even though it has not yet finished its current OPEN operation) so NFIRST_LOCKED is used to show that this is the first locked operation. During the first locked

operation, you do NOT want to compare the LOCKED_LRA with the current LRA because the LOCKED_LRA will be invalid.

RQ_BI_TI: T-Bus input interface for the Requestor. Latches and decodes current T-Bus data into the DEC_TBUS bus (pg. 63). Assembles logical and physical route address (pg. 64). Holds the Logical Route Address if the Requestor just becomes locked. Calculates FQ_VALID (pg. 64). Assembles the Switch message header data into the MSG_HEAD bus according to configuration settings (pg. 65).

When FQ_VALID is asserted (=1), the BIU is in IDLE [LOCKED] and is receiving a bus request. The exception to this is when the Requestor is locked and it receives a valid request from a master to which it is not locked. Basically, FQ_VALID tells the BIU when it can leave the IDLE [LOCKED] state. Normally, the Requestor would want to advance from IDLE with ANY T-Bus request and respond with a PROMISE. However, the T-Bus specification requires that a slave issue a REFUSED [LOCKED] without first issuing a promise. Therefore, FQ_VALID must be calculated as shown (on pg. 64).

XPRA_GEN: This is a maximum sequence generator which represents the equation:

$$X^{11} + X^{2} + 1$$

RQ_BI_CT: The Bus interface state machine is fairly straightfoward. The FQ_Anticipator (lower right of pg. 76) would normally be used to tell when to command the STU to begin transmission (BIU_EXECUTE). However, there is a bug which does not allow BIU_EXECUTE to be asserted during an interleaved read access (IFF Anticipator = 1XX). Basically, NSTE_SPAUSE_BR1 was not included in the FQ_Anticipator. Therefore, the anticipator must ALWAYS be set to 1XX.

RQ_SR: This is the Switch Receiver module. It handles the collection of all upstream messages.

RQ_SR_DA: Contains the receive register file for the Switch Receiver. Note on page 190, UDATA.* is a transparent latch used to give extra hold time to the RAM1 cells. On page 191 (left-half), the Stolen bit or Error bit is captured in its possible positions. Note that if either is received, the logic expects that byte to be the last of the upstream message. This is O.K. because the Server always ends a message when it encounters its first stolen bit. The right-half of page 191 detects the various Switch and Remote errors.

RQ_SR_CT: The Switch receive controller is fairly simple. It starts a pulse train down the RQ_ST_DA RAM1 enable logic when a message is believed to be entering the Requestor Switch interface. Note that the when a particular state in the State Machine is reached, the Switch data currently at the input latches is for the NEXT state. The Controller is held in reset while the STU is in IDLE (unlocked). This is just a saftey measure to insure the state of the SRU in case somehow the STU and SRU get out of sync.

RQ_IO: This is the I/O module for the Requesor Switch Transmitter. It is hierarchically separated from the rest of the logic for placement reasons.

RQ_TM: The Timer Module (a.k.a. Counter Module) contains the Switch transmission protocol logic, Synchronous Access Unit, and TONI/RTC logic. Creates the CNT_OUT bus which indicates the status of the various

counters. The 2-1 mux, U9, is used to seleect whether or not the slotted or random mechanism is being used.

RQ_TM_SU: The Synchronous Access Unit is used for accesses to RQ_TM sub-modules which must be synchronized to the One Microsecond clock period. It simply waits for an EXECUTE command, then waits for the next OMSP. When that event occurs, the SAU creates a strobe pulse (used in TONI/RTC write operations) and returns a COMPLETED status. The SAU interfaces with CS_CT. The CS_CT issues an execute to the RQ_TM_SU whenever it detects the following: 1) a write to TONIA/B (Config or Data), or 2) a read or write to the RTC. U19, U32, and U34 on page 98 detect a synchronous access.

RQ_TM_PT: Priority Time Slot detector. Simply an equality detector which is updated every OMSP.

RQ_TM_RR: Random Start/Retry module. Contains the exponent adder and mask generator described in the Siga Specification. U16 provides a bypass to the pipeline of U15 when the FIRST random backoff mask must be loaded. After that U15 is used.

XRSR_RND: This is a maximum sequence generator which represents the equation:

$$X^{15} + X^{4} + 1$$

XRSR_BOC: Backoff Counter. This counter uses a "minus one" detect to ease testing. It also uses a parallel carry because it must resolve the carry in one Switch Interval when it is loaded with a new value.

RQ_TM_RP: Real Time Prescaler. This module pipelines SFMSP and OMSP for use by other modules. URTP_5 is used to ensure that OMSP has a 50% duty cycle. This is important only for the Slotted Start/Retry mechanism.

RQ_TM_RJ: Reject Timer. Used to detect Reject timeouts. This timer is held in reset by the RQ_ST_CT just before the initial transmission (STE_IDLE, STE_HOLD).

RQ_TM_CO: Connection Timer. This is reset just before initial transmission and after every Reject is received.

RQ_TM_TS: TONI subtraction Unit. This is updated every OMSP.

XTONI_SB: This is the actual TONI subtractor. It is a 32-bit subtractor broken into two 16-bit halves. Since RQ_TM_TS only needs to detect when the equation, "TONI minus RTC" is negative, only the borrow is calculated - until the very last stage.

RQ_TM_RC: The Real Time Clock. Just a 32-bit up-counter.

RQ_TM_SR: Slotted Retry. Does the comparsion described in the SIGA Specification.

CS_CT: Configuration Status Unit controller. Errors are detected during the Function Request. The SAU_COMPLETED signal is put through a discrete fixed-delay synchronizer other than XSYNC_FX because this gives a smaller "round-trip" delay to the SAU. The SAU also employs this type of synchronizer - although it has a 4 clock settling time. The round-trip delay must be less than 1 us, otherwise synchronized accesses may trash the read/write data.

TI_CT: The T-Bus Interface Unit handles the T-Bus arbitration between the Requestor, Server, CSU, TCU and the T-Bus. It has a "fast" path for calculating the next data and driver of the T-Bus. This fast path uses as its input just enough T-Bus signals to make its calculation. The path has NO input hold latches and relies on natural data path decay (plus T-Bus hold time) to give it hold-time at the output pipeline registers in TI_DA.

This also calculates, in parallel, the data Bus Requests and Bus Grants for the other high-level modules in the SIGA (pg. 12). Also on page 12, is the "next response" logic of the RQ_BI_CT while in STE_IDLE. This is placed in the TIU mainly for speed considerations during layout. On page 13, U35 and U36 are used to allow the CSU to modify the TDAT/TRANS fields while being read. This is because the CSU always issues a pause when it is being accessed and it MUST be able to modify its data.

TI_CT_SH: Sample and hold module for "look-ahead" calculation of next SIGA-to-TBUS data/enables.

TI_CT_DT: Detects the CSU map present on the T-Bus.

TI_DA: Data module for the TIU. It is separated hierarchically mainly for layout.

SV_IO: Data module for the Server. It is separated hierarchically mainly for layout.

SV_ST_CT: Server Switch Transmitter Controller. Generates Rejects and control signals for the SV_ST_DA. Those signals allow the SV_ST_DA to assemble Switch messages after T-Bus accesses.

SV_ST_DA: Calculate checksum. Append checksum and possible error codes to the message.U2 ensures that valid data is loaded into the XTX_SRLZ in the event that the T-Bus response was not driven. This ensures that the checksum will be calculated correctly in the event of a "no response" on the T-Bus.

XTX_SRLZ: Server Transmit data serializer.

SV_SR_DA: Receive the downstream message. Calculate the checksum and flag a bad checksum. RX_ANT is the receive anticipator signal. It is true exactly five clock ticks before the checksum during writes and during Address word #3 on reads. RX_CS_OK is a pulse, GOT_BAD_CS is a level.

SV_SR_CT: Switch receive state machine. NNOC_SOC allows the Server to refuse (by rejecting) the start of a new connection. This is the "graceful" method of preventing new connections.

SV_CN: Server configuration registers.

***End of request Q00000.19104 for plevin@cheese.bbn.com Mon Aug 15 11:51:15 1988

***End of request Q00000.19104 for plevin@cheese.bbn.com Mon Aug 15 11:51:15 1988

Printed on queue freshqms, device freshqms
12 pages of output
1 file printed
Used 1210 milliseconds of runtime

***End of request Q00000.19104 for plevin@cheese.bbn.com Mon Aug 15 11:51:15 1988

***End of request Q00000.19104 for plevin@cheese.bbn.com Mon Aug 15 11:51:15 1988

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(a) VTI Parameters

NOTES: Using the VTG100-270, which is a 20k used gates part
Numbers are based on worst-case process, Vdd=4.5, 85 degrees C junction temp (70 deg C ambient)
Delay Table is based on worst-case environment
Total Delay = Inertial+Intrinsic+(Load Dependent*Load Capacitance)
Load Capacitance = (Fanout*Standard Load) + (#nets*Load/Net)
The number of nets are the number of pins in a node
Load/Net is taken a confidence level of 70%, which is considered average
For delay data, worst-case of H-to-L and L-to-H is used

STD LOAD 0.18

LOAD/NET 0.147

DELAY TABLE (sort!!!!)

	Inertial	Intrinsic	Load Dependent
2-in AND	1.6	0.61	1.7
2-in NAND	0.5	0.76	2
2-in NOR	0.8	1.18	3.2
DFF-Q	6.5	0.44	1.2
DFF-Q*	5.2	0.58	1.6
DFF-SETUP	4	0	0

(b) LSI Parameters

NOTES: Using the LCA10051 which is a 20k used gates part
Numbers are based on nominal process
The multiplier for: Vdd=4.5, 85 deg C junction is: 1.15(V)*1.22(T)*1.5(P) = 2.1
Delay Table is based on nominal environment
Total Delay = Intrinsic+(Load Dependent*Load Capacitance)
Layout Loading = (Standard Load) + (Fanout*Standard Load/Fanout)
Fanout is the number of pins in a node minus one
Load/Fanout is taken a confidence level of 70%, which is considered average
Layout loading calculations:
The LCA10051 has 50,904 available gates
So, block size at 708 gates/mm is 50,904/708 = 71.9 mm
Which is about 8x8mm
Therefore, the 8x8 mm block has a slope of 1.59 and intercept of .245
Loading is done in terms of standard loads
For delay data, worst-case of H-to-L and L-to-H is used

ASIC Vendor Speed Comparison

VTI			LSI		
CELL	FANOUT	DELAY (a)	CELL	FANOUT	DELAY (b)
DFF-Q*	1	6.54	FD1-Q*	1	3.90
2-in NAND	1	2.21	ND2	1	1.58
2-in NOR	1	3.50	NR2	1	2.15
2-in NAND	1	2.21	ND2	1	1.58
2-in NOR	1	3.50	NR2	1	2.15
2-in NAND	1	2.21	ND2	1	1.58
DFF-SETUP	0	2.00	FD1-SETUP	1	1.68
Total Delay (ns)		22.16			14.63
DFF-Q*	2	7.06	FD1-Q*	2	4.39
2-in NAND	2	2.86	ND2	2	2.04
2-in NOR	2	4.54	NR2	2	3.02
2-in NAND	2	2.86	ND2	2	2.04
2-in NOR	2	4.54	NR2	2	3.02
2-in NAND	2	2.86	ND2	2	2.04
DFF-SETUP	0	2.00	FD1-SETUP	2	1.68
Total Delay (ns)		26.73			18.22
DFF-Q*	3	7.58	FD1-Q*	3	4.87
2-in NAND	3	3.52	ND2	3	2.50
2-in NOR	3	5.59	NR2	3	3.88
2-in NAND	3	3.52	ND2	3	2.50
2-in NOR	3	5.59	NR2	3	3.88
2-in NAND	3	3.52	ND2	3	2.50
DFF-SETUP	0	2.00	FD1-SETUP	3	1.68
Total Delay (ns)		31.31			21.82
DFF-Q*	4	8.11	FD1-Q*	4	5.36
2-in NAND	4	4.17	ND2	4	2.96
2-in NOR	4	6.64	NR2	4	4.75
2-in NAND	4	4.17	ND2	4	2.96
2-in NOR	4	6.64	NR2	4	4.75
2-in NAND	4	4.17	ND2	4	2.96
DFF-SETUP	0	2.00	FD1-SETUP	4	1.68

Total Delay (ns)		35.89			25.41
DFF-Q*	5	8.63	FD1-Q*	5	5.85
2-in NAND	5	4.82	ND2	5	3.42
2-in NOR	5	7.68	NR2	5	5.61
2-in NAND	5	4.82	ND2	5	3.42
2-in NOR	5	7.68	NR2	5	5.61
2-in NAND	5	4.82	ND2	5	3.42
DFF-SETUP	0	2.00	FD1-SETUP	5	1.68
Total Delay (ns)		40.47			29.01

COSTS RELATED TO FIRST ARRAY (YEAR 1)

DEVELOPMENT

	VTI		LSI	
S/W Tools	$61,750	(a)	S/W Tools	$60,000 (c)
Maintenance	$6,930	(a)	Maintenance	
NRE	$64,500	(b)	NRE	$89,500 (d)
Total	**$133,180**		Total	**$149,500**

PRODUCTION

	VTI (b)		LSI (d)	
	@ 5k	@10k	@ 5k	@ 10k
Piece Price Plastic	$93.23	$89.93	(e)	(e)
Piece Price Ceramic	$130.87	$124.68	$110.51	$103.84
Total Plastic	**$466,150**	**$899,300**	(e)	(e)
Total Ceramic	**$654,350**	**$1,246,800**	**$552,550**	**$1,038,400**

INCREMENTAL COSTS FOR SECOND ARRAY (YEAR 2) (g)

DEVELOPMENT

	VTI		LSI	
S/W Tools			S/W Tools	$257,000 (f)
Maintenance	$6,930	(a)	Less applied License	($60,000)
			Less discount ??	($30,000)
Total	**$6,930**		Maintenance	$39,800 (f)

			Total	$206,800

INCREMENTAL COSTS FOR THIRD ARRAY (YEAR 3) (g)

DEVELOPMENT

	VTI			LSI
S/W Tools			S/W Tools	
Maintenance	$6,930	(a)	Maintenance	
Total	**$6,930**			**$0**

Total non-NRE dev costs for 3 years	$82,540	$266,800

MULTIPLIER 2.10

FANOUT LOADING

Load/Fanout	1.59
Standard Load	0.245

DELAY TABLE (sort!!!!)

	Intrinsic	Load Dependent
AN2	0.48	0.1443
AN2P	0.54	0.0718
FD1-Q	1.09	0.1458
FD1-Q*	1.59	0.1458
FD1-SETUP	0.8	0
FD1P-Q	1.16	0.0653
FD1P-Q*	1.84	0.0669
ND2	0.5	0.1377
ND2P	0.5	0.0623
NR2	0.55	0.2589
NR2P	0.56	0.1282

NOTES

(a) VTI tools costs

	License Fee	Annual Maintenance
VTI S/W package	$35,000	$4,200
2.0u G.A. lib		
1.5u G.A. lib		
2.0u G.A. lib		
2.0u compiler lib		
Installation		
Training	$4,000	
One additional node	$22,750	$2,730
Total	**$61,750**	**$6,930**

(b) Quoted for a VTG100-270, 20K used gates, 10 ceramic protos. Ceramic is NOT high-performance

(c) Special License, good for one design only. Limit of one year

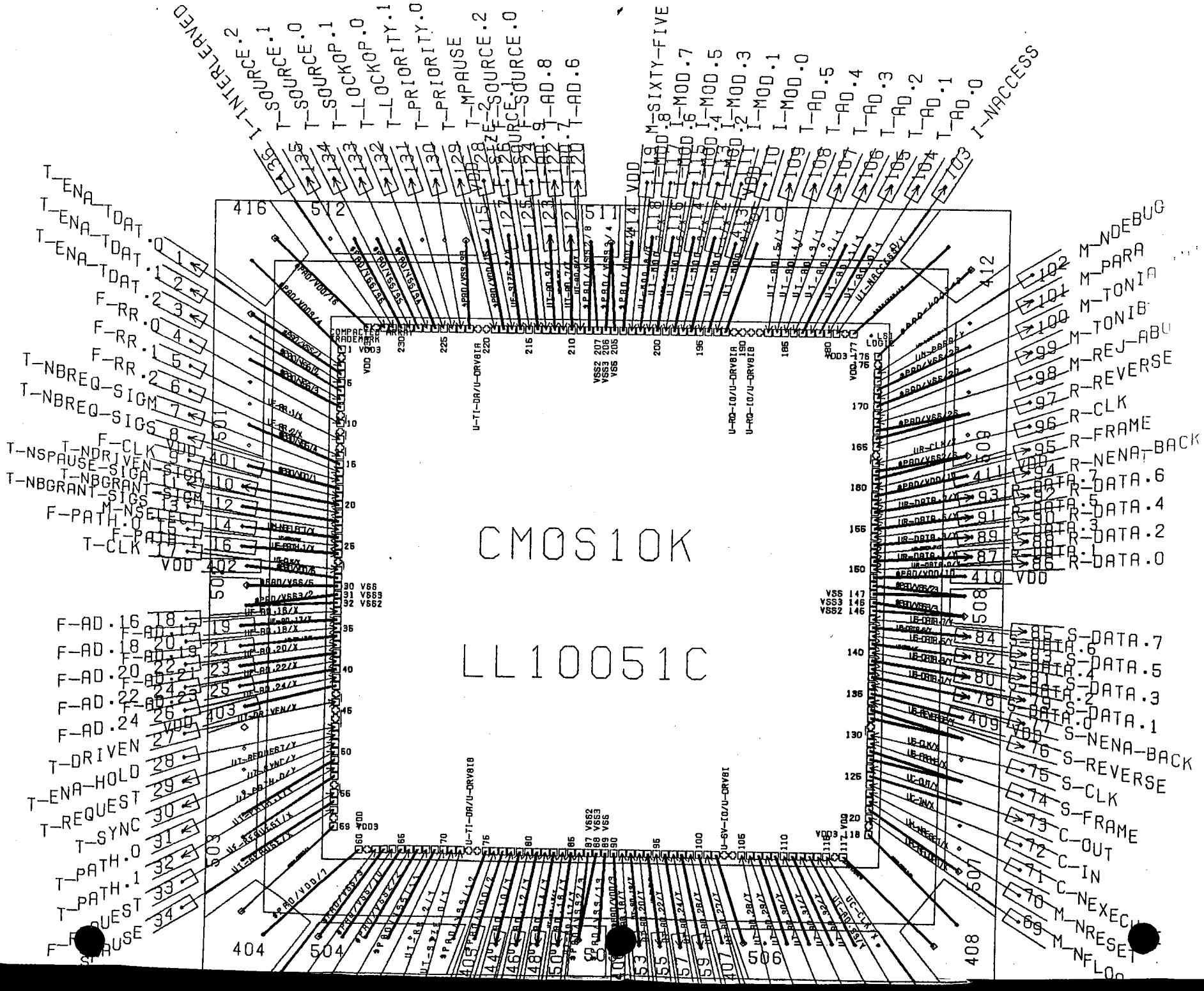
(d) Quoted for a LCA10051, 20K used gates, 10 ceramic protos. Production in a 155 CPGA (high-performance)

(e) LSI does not recommend plastic for this array size

(f) LSI tools cost

	License Fee	Annual Maintenance
LDS III	$65,000	$11,700
LDS Graphics	$15,000	$2,700
LCA 10000 Library	$80,000	$14,400
MEGALCA Library	$50,000	$9,000
Installation?	$5,000	
One additional node	$42,000	$2,000
Total	**$257,000**	**$39,800**

(g) Does not include new NRE's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F-RR.2
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T-NBREQ-SIGS
F-CLK
T-NSPAUSE-SIGA
T-NBGRANT-SIGM
T-NBGRANT-SIGS
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F-PATH.1
T-CLK
F-AD.16
F-AD.17
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F-AD.20
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F-AD.24
T-DRIVEN
T-ENA-HOLD
T-REQUEST
T-SYNC
T-PATH.0
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T-SOURCE.0
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I-MOD.2
I-MOD.1
I-MOD.0
T-AD.5
T-AD.4
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T-AD.2
T-AD.1
T-AD.0
I-NACCESS
M-NDEBUG
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M-TONIA
M-TONIB
M-REJ-ABU
R-REVERSE
R-CLK
R-FRAME
R-NENA-BACK
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R-DATA.6
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S-DATA.5
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S-DATA.3
S-DATA.2
S-DATA.1
S-DATA.0
S-NENA-BACK
S-REVERSE
S-CLK
S-FRAME
C-OUT
C-IN
C-NEXEC
M-NRESET
M-NFLOO
VDD
VSS
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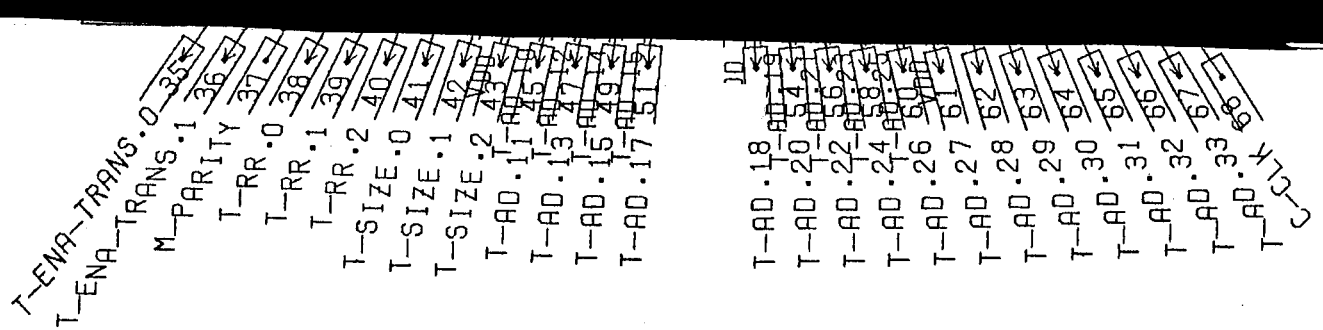


L1A3496 WALT MH AY FDEX

DATE RELEASED: TUE MAY 31 13:42:25 1988

BDCMD TIME: SUN MAY 29 22:25:19 1988

DESCRIPTION

155 CPGA 0.470 CAVITY

BONDING DIAGRAM NOTEPAD

PACKAGE CODE = FR47

DIE SIZE = 9.900MM X 9.900MM

APPROVALS:

ENG Mark J. Halbert *

PKG _____ *

QA _____

CUST C-P Philip Fan

JUN 10 1988

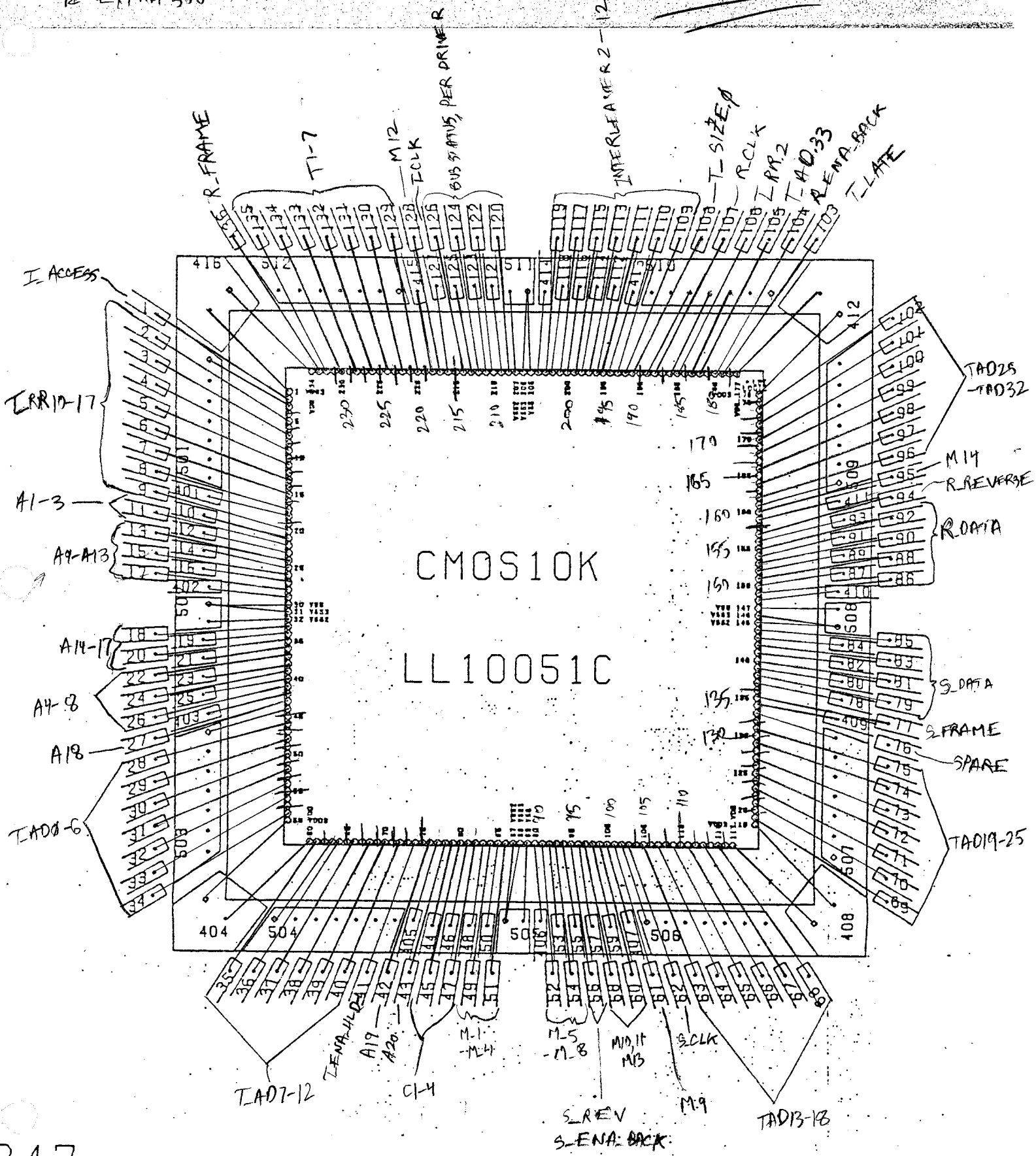
DOC. #

PAGE OF

12 EXTRA 400

12 EXTRA 500

PASS #1

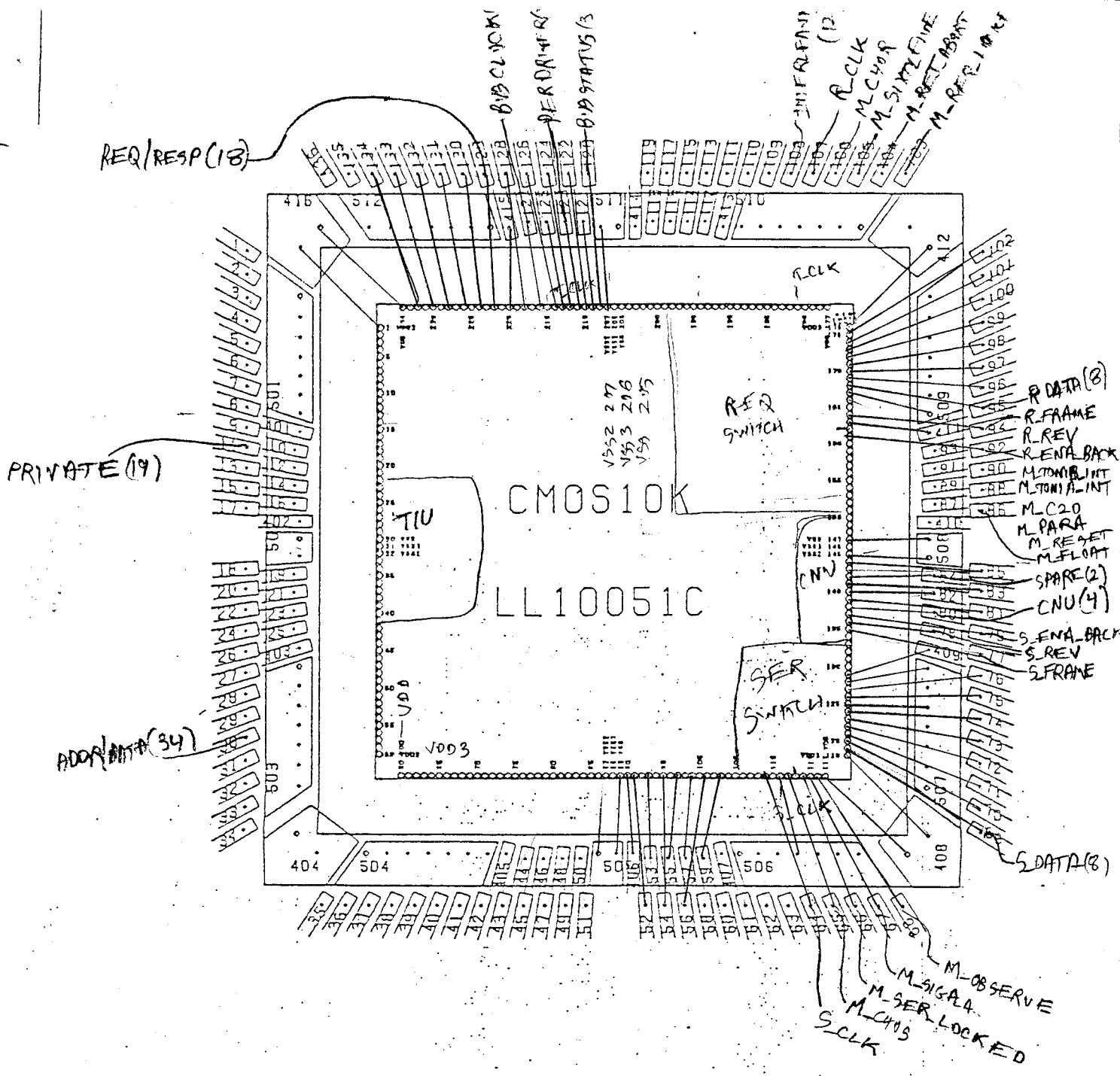


FR47

ATE RELEASED: THU FEB 12 14:35:44 1987

DESCRIPTION

155 CPGA 0.470 CAVITY



FR47

DATE RELEASED: THU FEB 12 14:35:44 1987

DESCRIPTION

155 CPGA 0.470 CAVITY

PACKAGE CODE FR47 FACTORY PART NO. _____ APPROVALS:

PKG. NO. _____ DIE SIZE 9.654MM X 9.660MM ENG _____

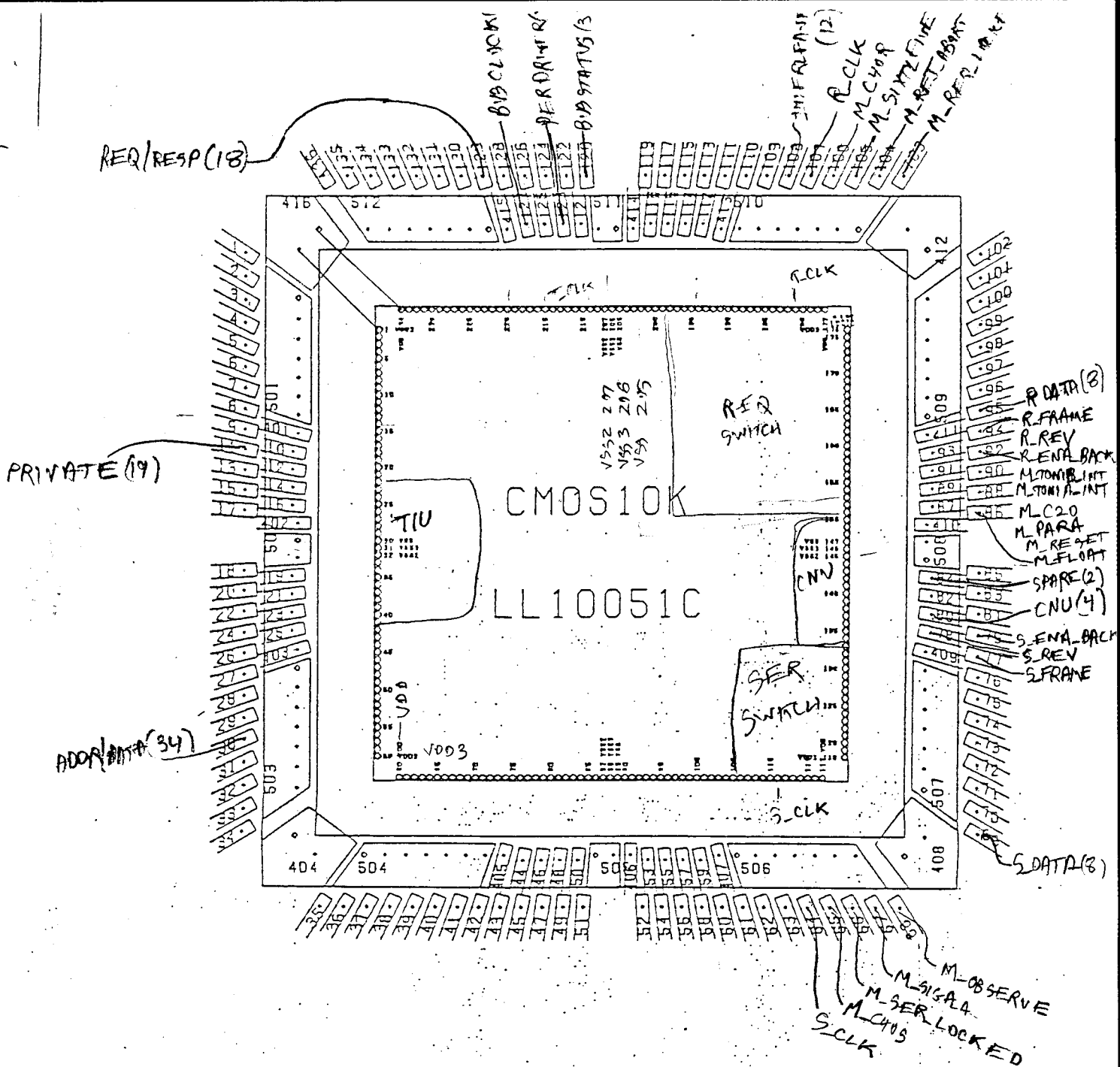
LID NO. _____ JUMPER CHIP: PKG _____

WIRE ALLOWED: REQUIRED _____ QA _____

ALUMINUM _____ OPTIONAL _____ CUST _____

5- VSS

4- VDD



FR47

DATE RELEASED: THU FEB 12 14:35:44 1987

DESCRIPTION

155 CPGA 0.470 CAVITY

PACKAGE CODE FR47 FACTORY PART NO. _____ APPROVALS:

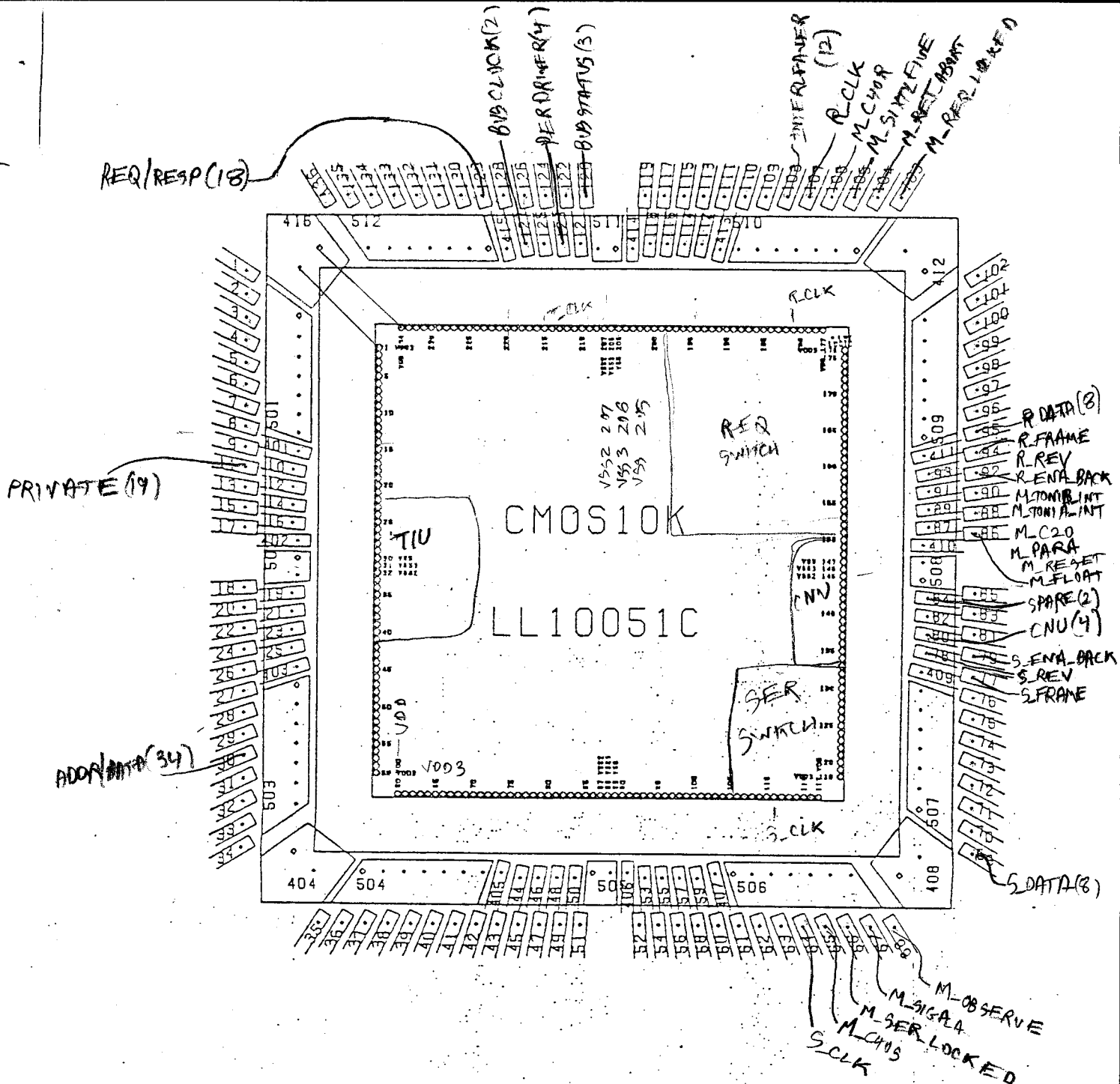
PKG. NO. _____ DIE SIZE 9.654MM X 9.660MM ENG _____

LID NO. _____ JUMPER CHIP: PKG _____

WIRE ALLOWED: REQUIRED _____ QA _____

ALUMINUM _____ OPTIONAL _____ CUST _____

5- VSS
4- VDD



FR47

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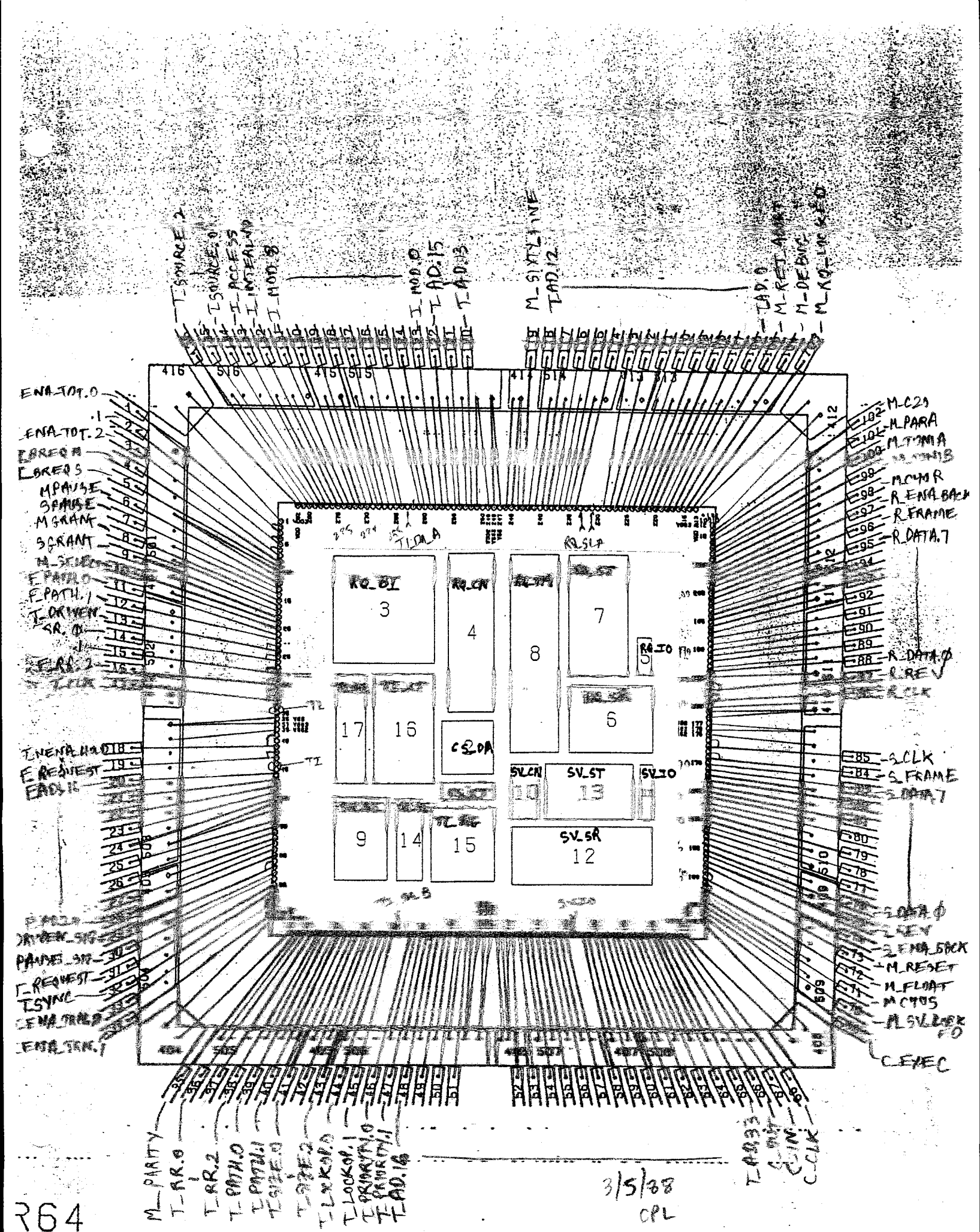
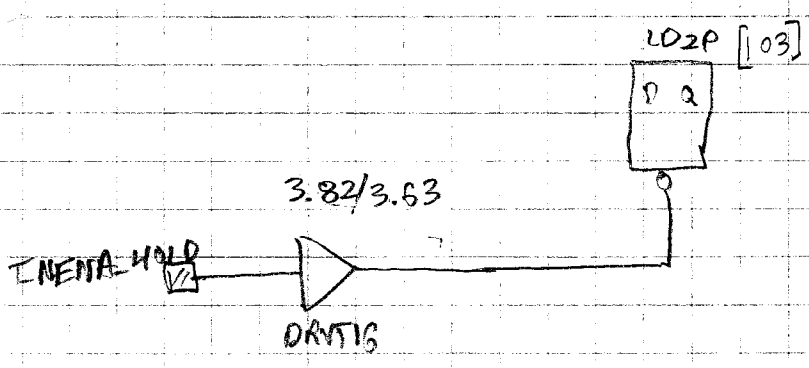
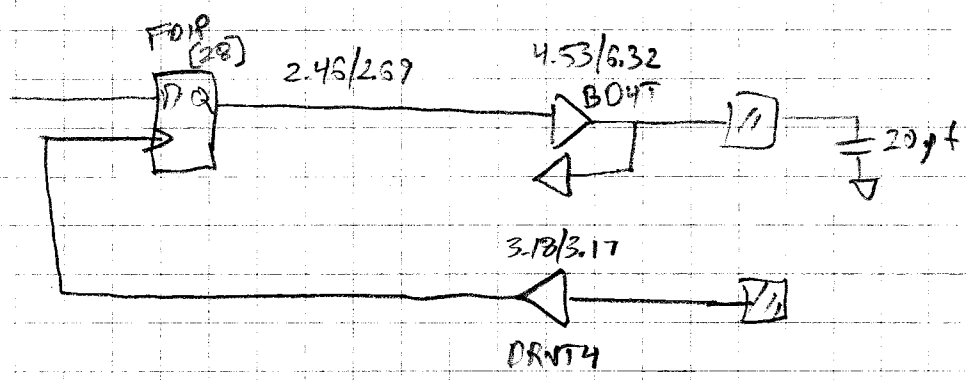
5 - VSS

4 - VDD


RQ_BI
3
RQ_CN
4
8
7
RQ_IO
5
6
17
16
CSDA
SVLCN
SV_ST
SVLIO
10
13
9
14
15
SV_SR
12
T_SOURCE.2
T_SOURCE.0
T_ACCESS
T_MOD.0
T_AD.15
M_SIXTYFIVE
TAD.12
TAD.0
M_RET_ABRT
M_DEBUG
M_KOTLIN_ED
ENA_TOT.0
ENA_TOT.2
BREQM
BREQS
MPAUSE
SPAUSE
MGRANT
SGRANT
M_SCLKEN
F_PATH.0
F_PATH.1
T_DRIVEN
SR.0
F_RR.2
T_CLK
T_ENA_HOLD
F_RESYNC
EAD.16
M_C29
M_PARA
M_TMA
M_C4B
M_C4R
R_ENA_BACK
R_FRAME
R_DATA.7
R_DATA.0
R_REV
R_CLK
S_CLK
S_FRAME
S_DATA.7
S_DATA.0
S_REV
S_ENA_BACK
M_RESET
M_FLOAT
M_C40S
M_SVLCK
C_REC
M_PARITY
T_RR.0
T_RR.2
T_PATH.0
T_PATH.1
T_SIZE.0
T_SIZE.2
T_LOCKOP.1
T_LOCKOP.0
T_PRIORITY.1
T_PRIORITY.0
T_LAD.16
T_AD.3
C_CLK
3/5/88
CPL
DIE SIZE = 11.458 MM X 11



HOLD LATCHES

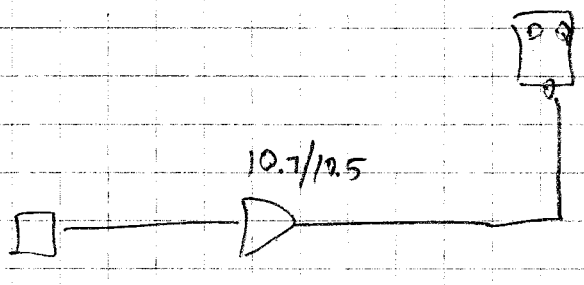


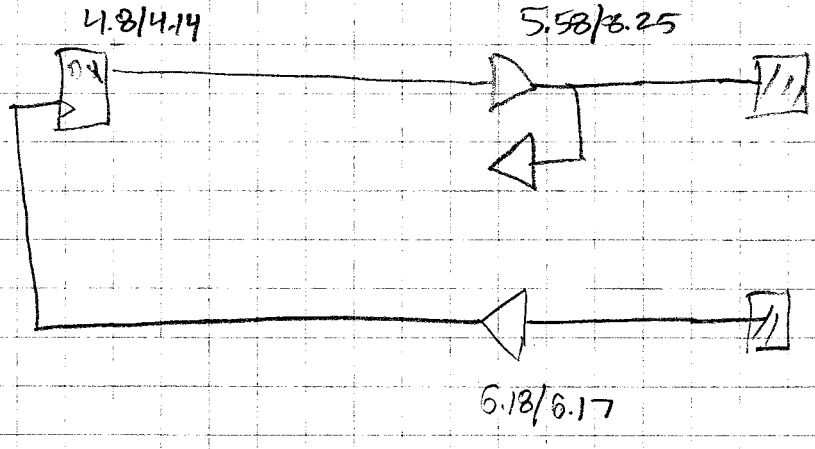
SERVER SWITCH I/F

ROUND TRIP = 10.7/12.2

REQUIREMENT: < 13.7 ns

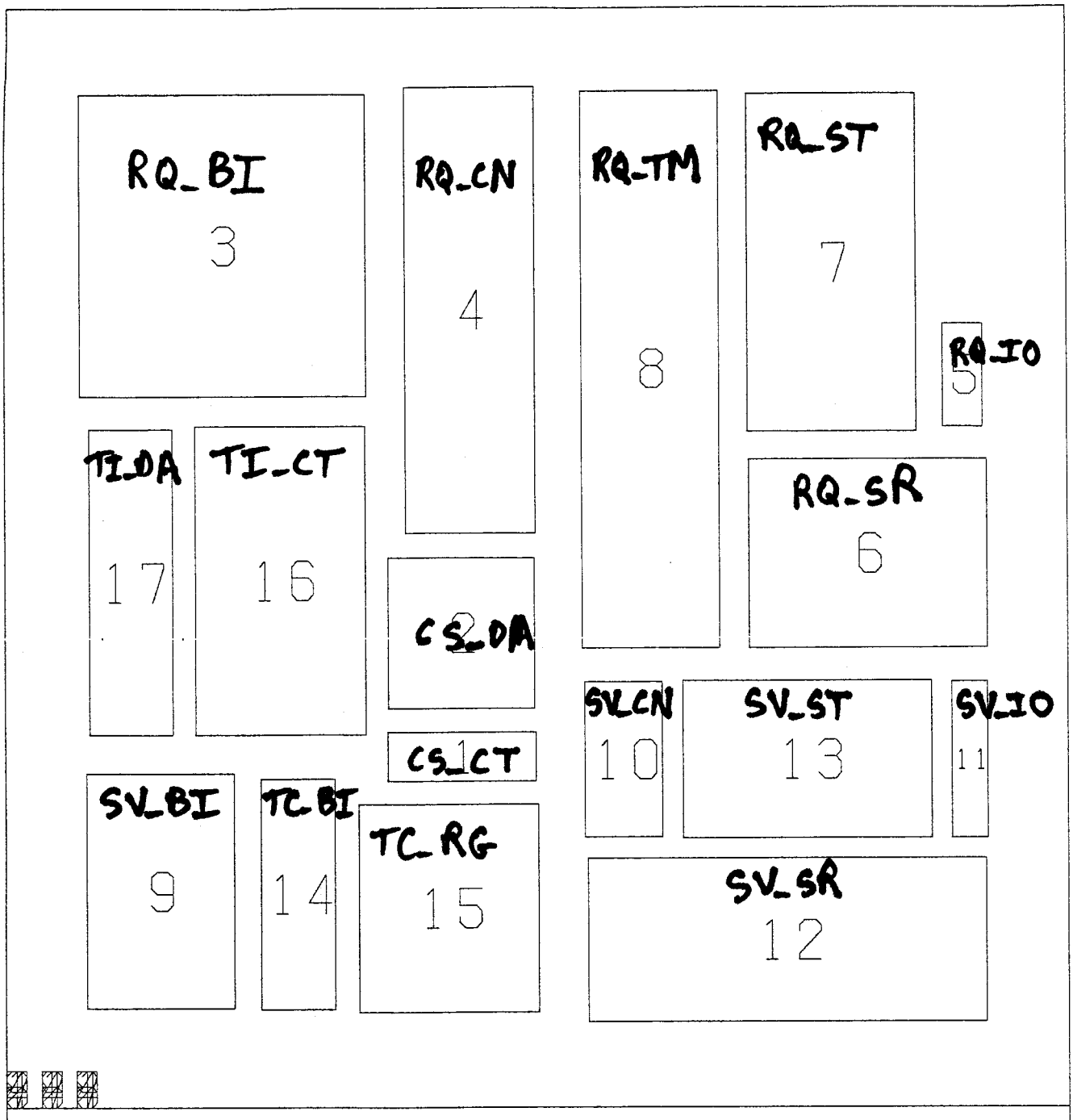
WITH FLATENED DELAYS





ROUND TRIP = 16.5/18.6

WITH LPACE DELAYS



DESIGN NAME : BBN

PROJECT ID : BBN

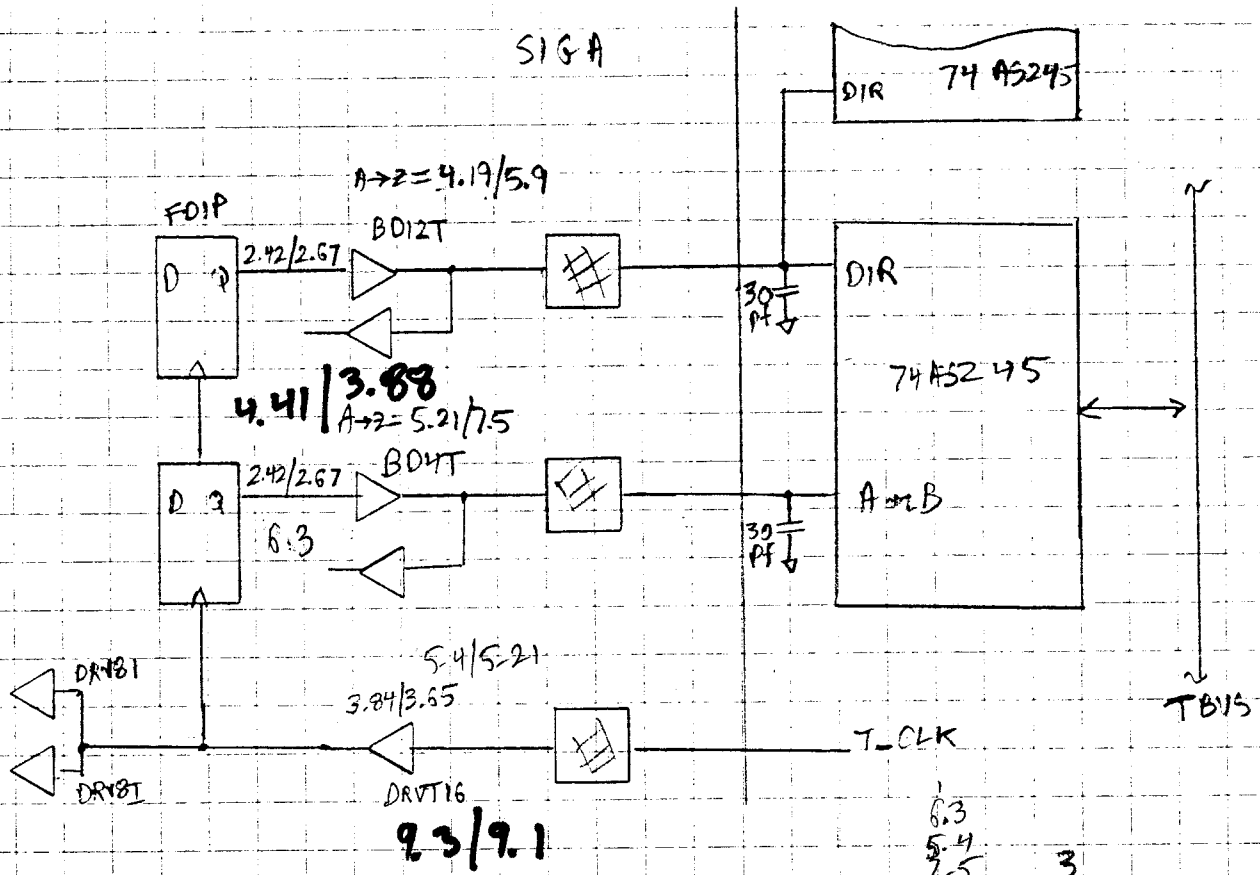
TOP MODULE : SIGA

TOTAL NUMBER OF NETS : 5599

PINS PER NET : 3.50

ROUTABILITY OF THE CHIP : 98 %

UTILIZATION OF THE CHIP : 20.24



6.3
5.4
7.5 3
19.2

16.2
2.5
23.7

LOADING:

	DIRECTION	DATA
AS245	= (2)(8 pf) = 16	16 pf
PC TRACE	12	12
	~30 pf	~30 pf

'AS245 CAPACITANCE:

DIR = 8 pf MAX

A or B = 16 pf MAX

PC TRACE CAPACITANCE:

(4 pf/inch)(3 in) = 12 pf

DELAY:

TCLK → FDIP-Q = 3.84 + 2.67 = 6.51

SO,

DATA = 6.51 + 7.5 + 7.5* = 21.5 ns

5.4 +
4.0
7.5
6.2
23.1

DIRECTION = 5.51 + 5.9 + 9.5* = 21.9 ns

*FROM TI AS245 SPECS

SIGA (DESIGN) TBUS I/F TIMING

1/6/87 CPL

3.95 / 5.45 4.18/3.73 3.95/5.45

5.13/4.94

AGENDA FOR MEETING WITH NEBULA

- SIGA design description
  - Basic structure
  - Current stage of design
  - Clocking scheme
  - Floorplan

- Discussion of problems encountered
  - Die size limitations
  - Speed problems with the larger die

- Specific Questions

  - SIGA speed
    - Is the LPACE delay estimation accurate?

  - SIGA routability
    - Is the LPACE Routability index accurate?
    - Is 75% routable acceptable?

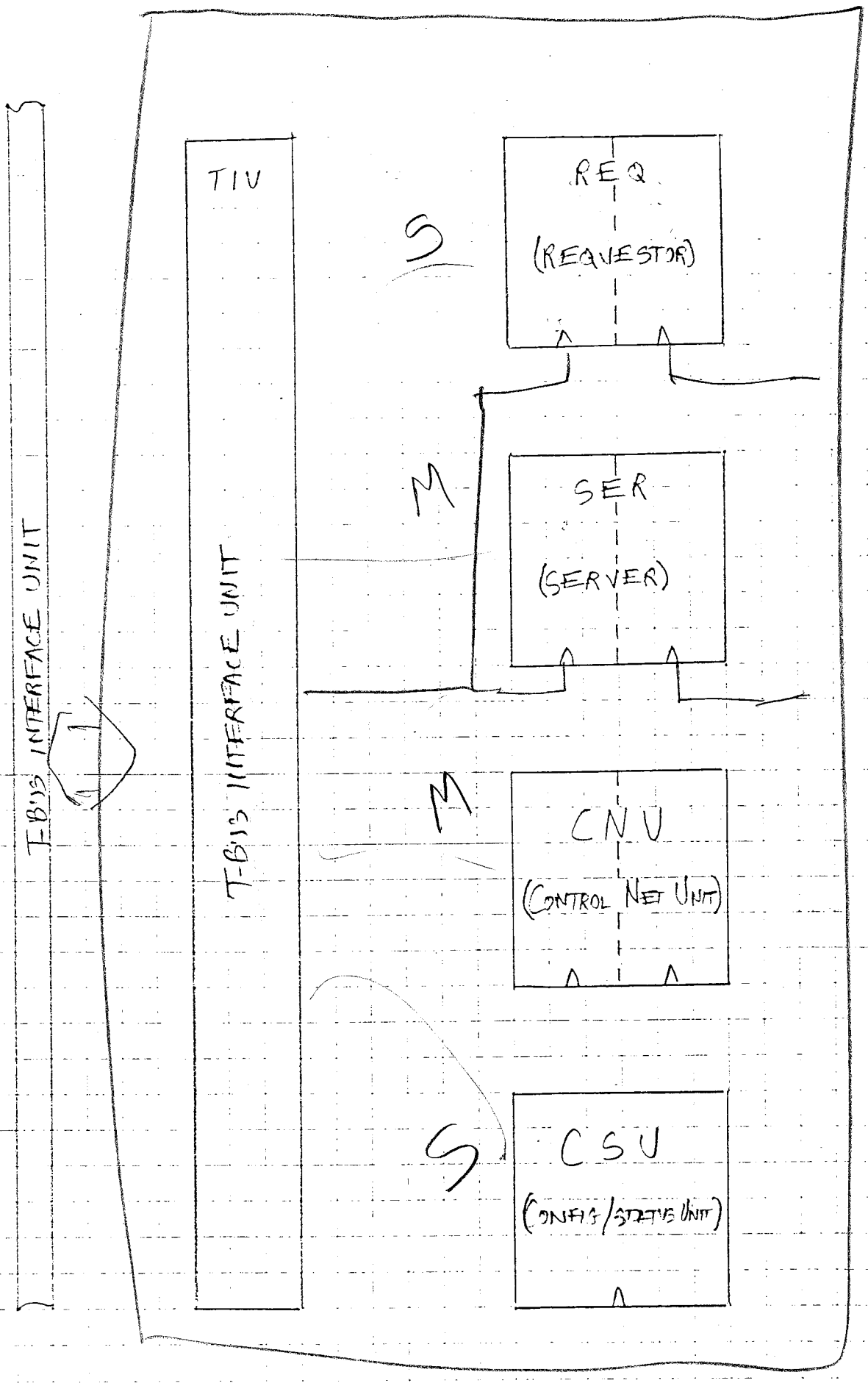
  - SIGA clocking scheme
    - Will LSI get it right?
    - What can be done to guarantee fast enough clock-to-q's?
    - What the best way to identify critical nets?

  - LCAP questions from Guy

  - Turn-around time
    - What is reality?

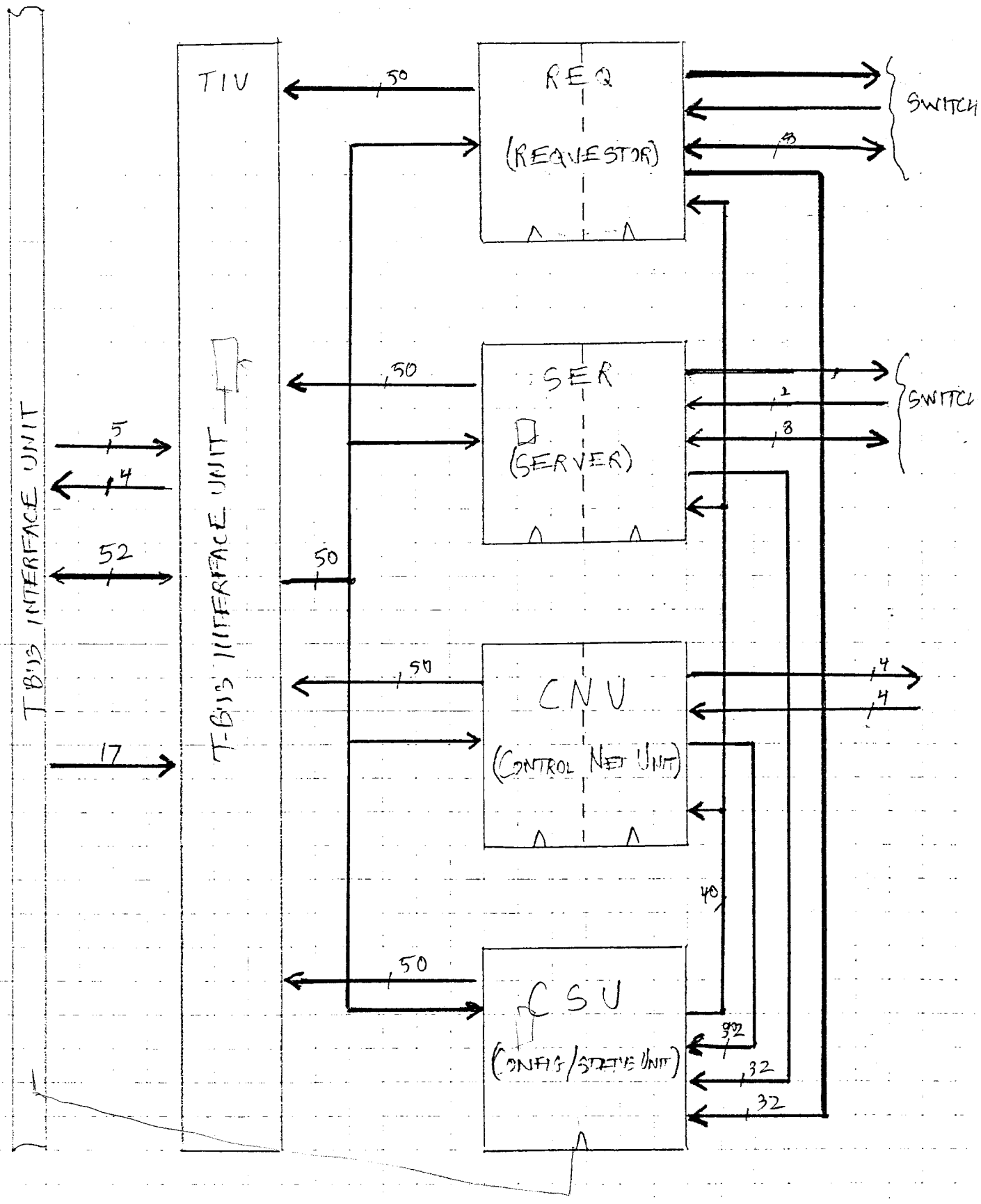
  - General
    - general pitfalls to avoid

WED @ 9AM MARK



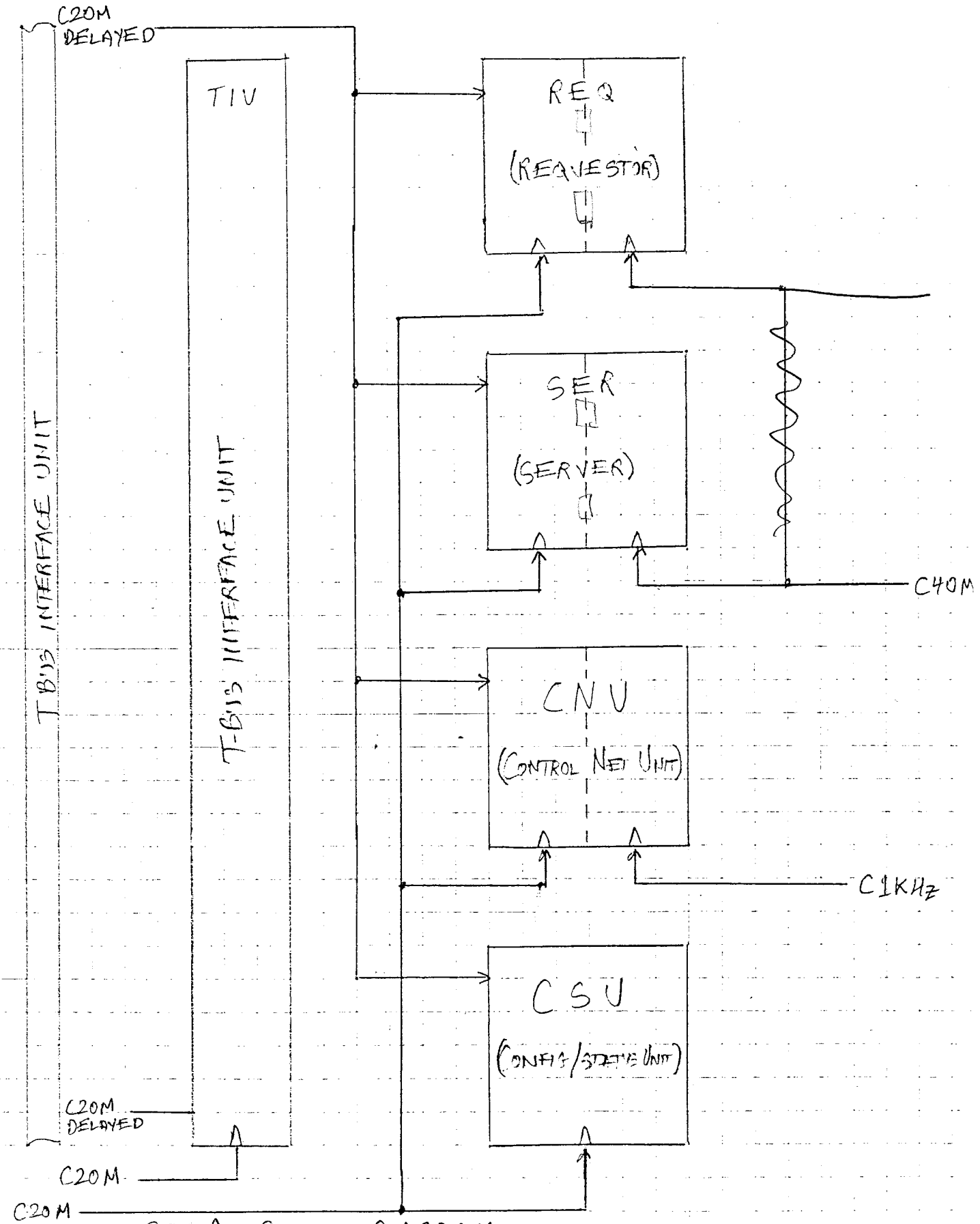
SIGA BLOCK DIAGRAM

10/3/57 CPL



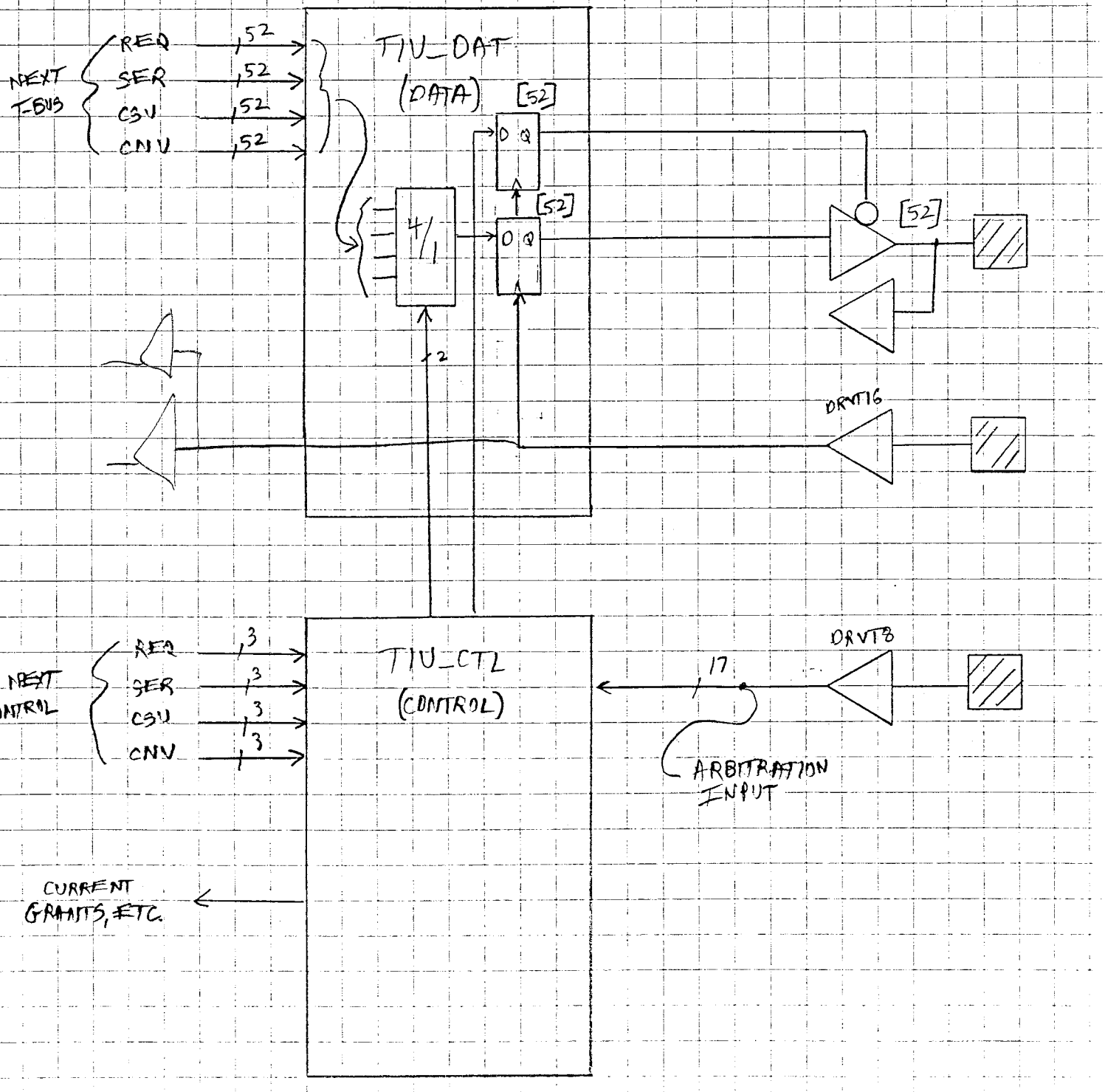
SIGA BLOCK DIAGRAM

INTERCONNECT



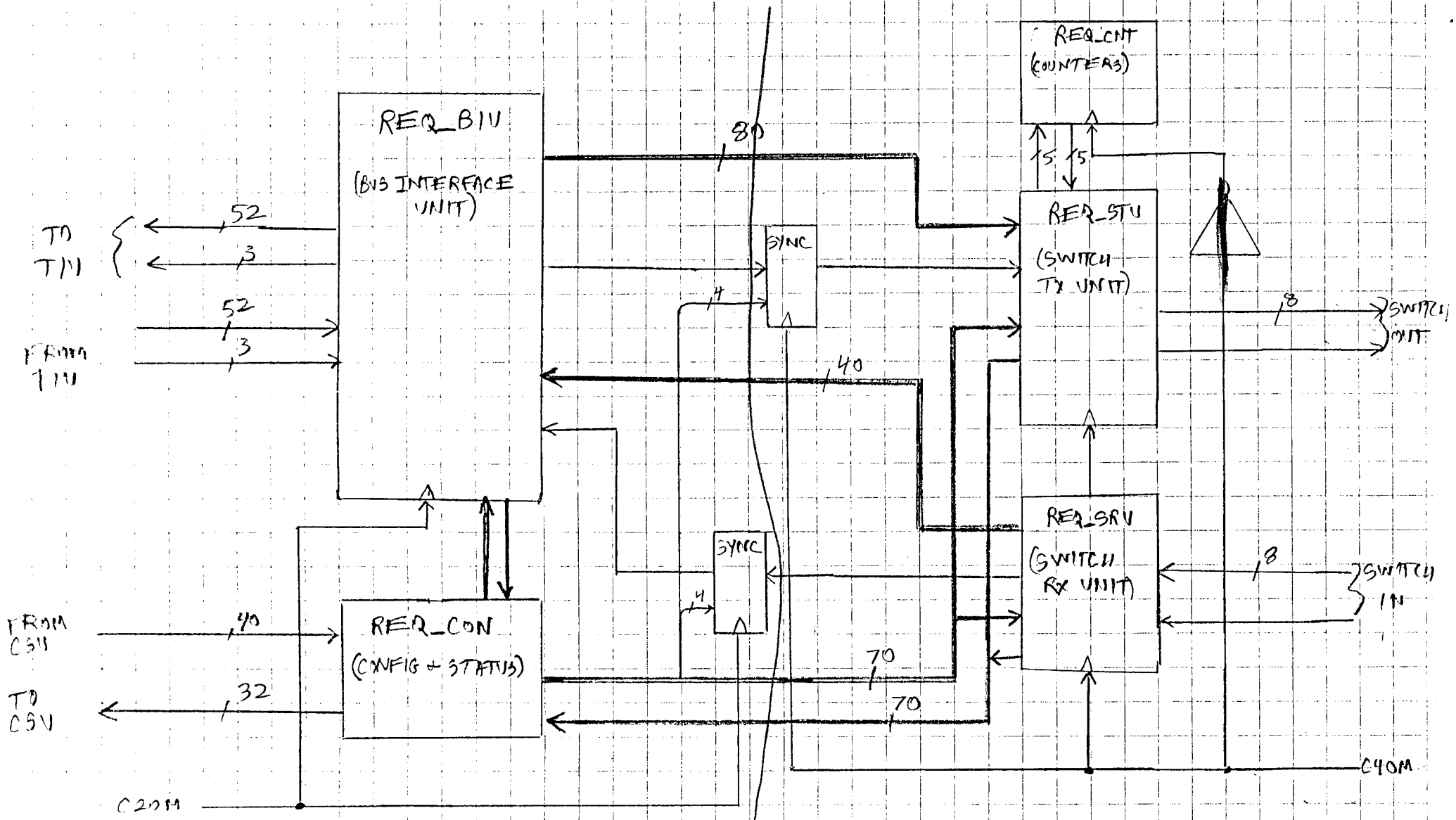
SIGA BLOCK DIAGRAM

CLOCKING



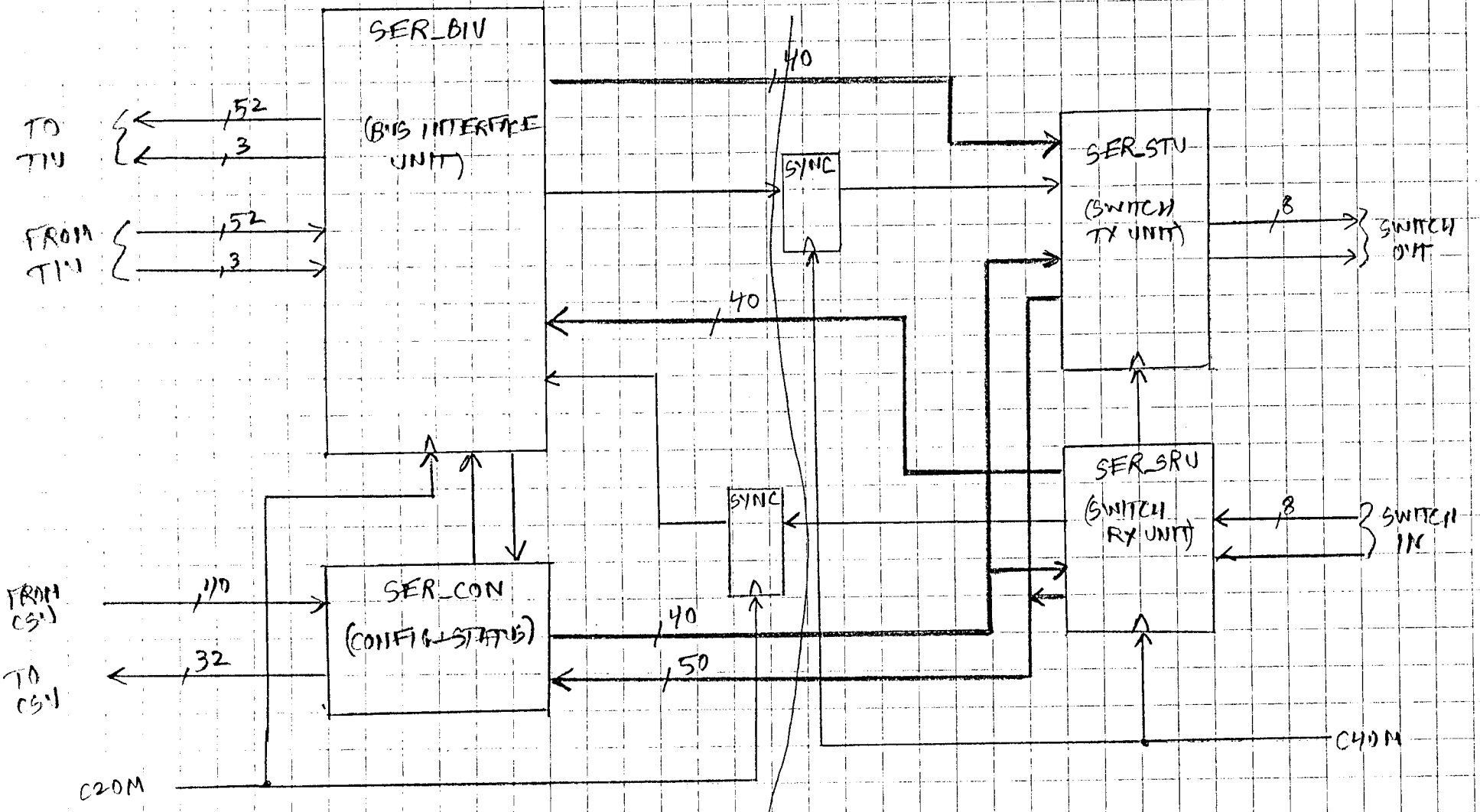
TIU BLOCK DIAGRAM

10/2/87 CPL



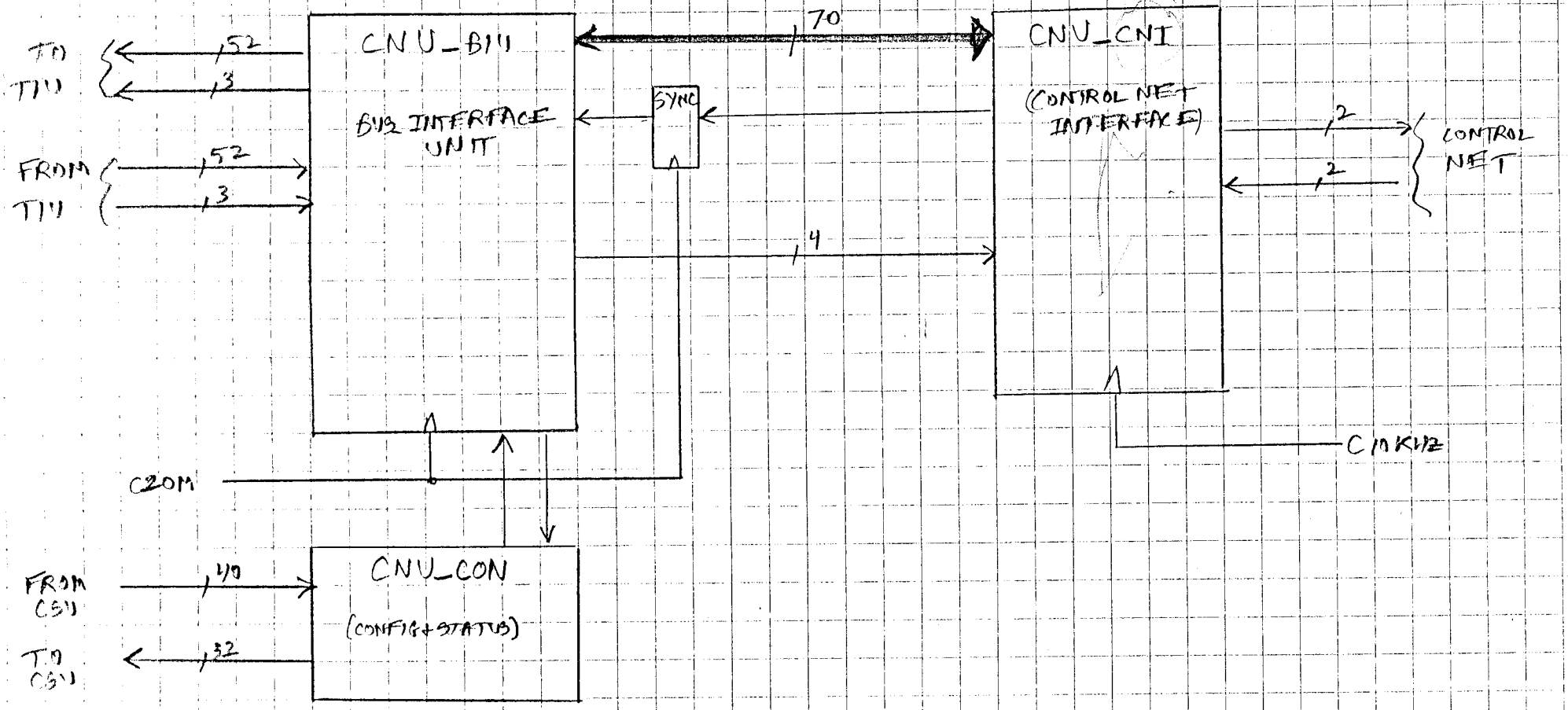
REQ BLOCK DIAGRAM

10/8/87 CPL



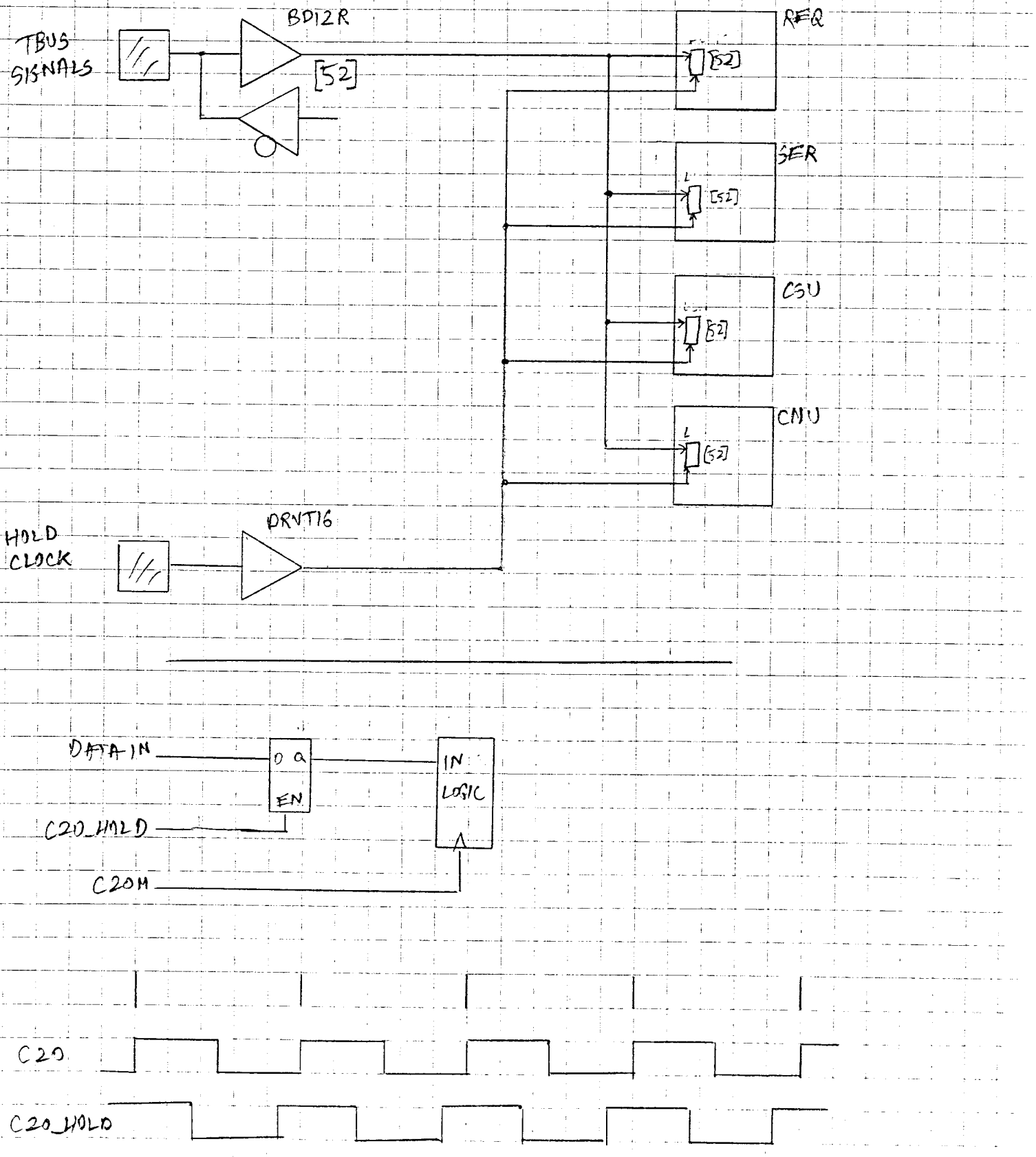
SER BLOCK DIAGRAM

10/2/87 CPL



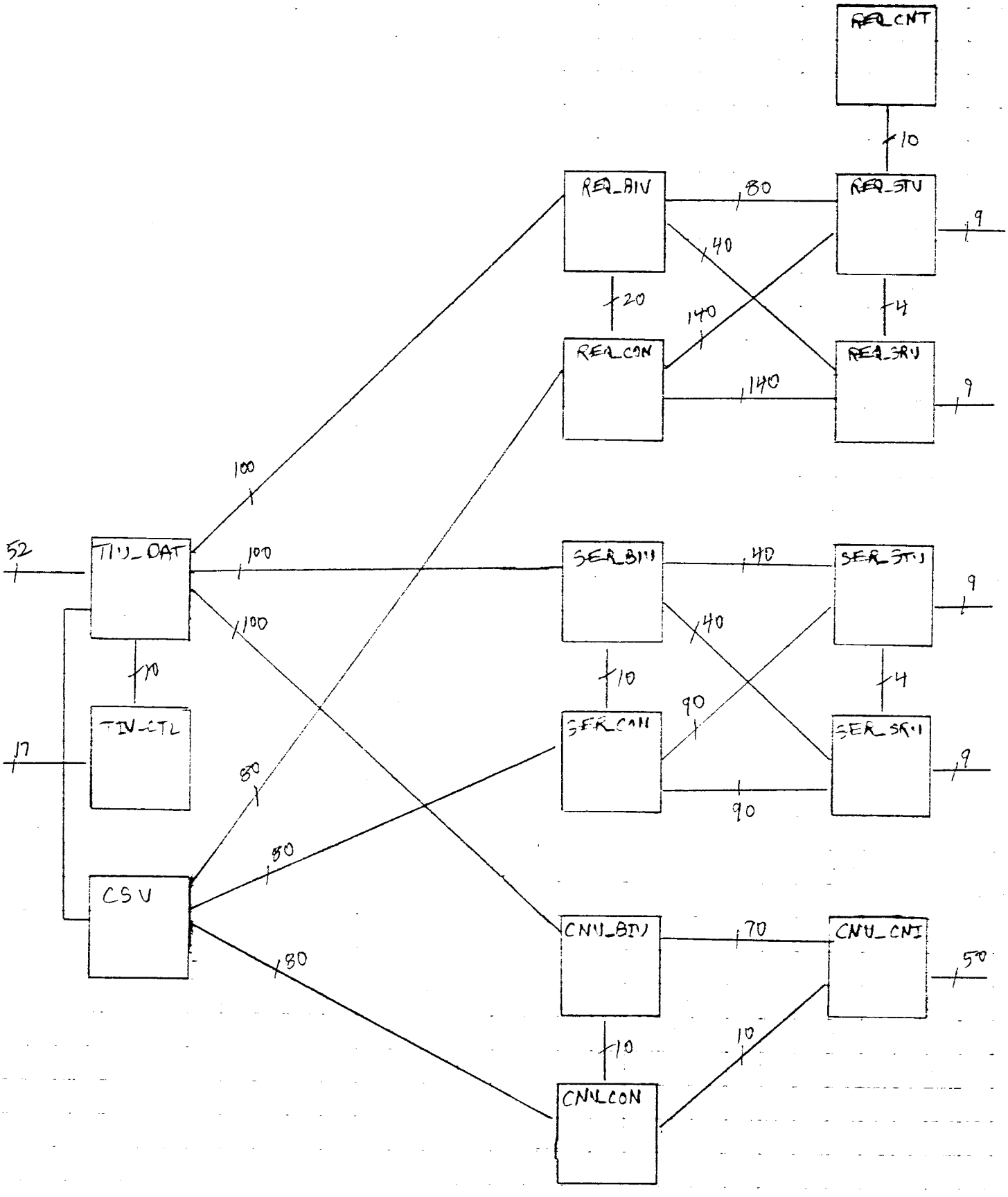
CNU BLOCK DIAGRAM

10/8/87 CPL



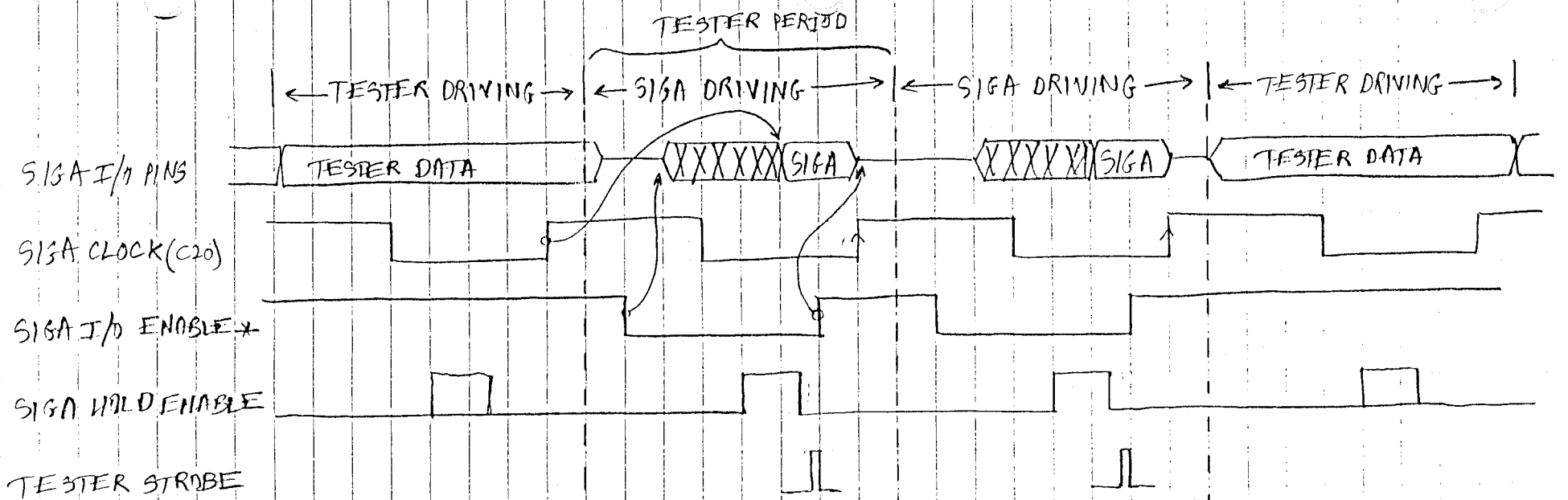
TBUS INPUT HOLD SCHEME

10/3/87 CPL



SIGA TOP LEVEL BLOCK INTERCONNECT (ESTIMATED

10/3/87 CPL



NOTE: SIGA I/O ENABLE IS ASSERTED ONLY DURING A TESTER PERIOD WHEN SIGA IS KNOWN TO BE DRIVING — maybe not!! 7/26/87

SIGA - CONCEPT - TESTER I/O CONTENTION SOLUTION

7/8/87 CPL

LDS3 VERIFIER STATISTICAL SUMMARY

LDS-III DESIGN VERIFIER NETWORK SUMMARY

PROJECT ID:	philsSIGA	LDS ACCOUNT NAME:	plevin
ARRAY NAME:	SIGA	ARRAY FAMILY:	CMOS10K
ARRAY TYPE:	LL10051C		
CURRENT DATE:	12/06/87	CURRENT TIME:	17:39:24
CMOS10K LIBRARY DATE:	06/15/87	CMOS10K LIBRARY REVISION:	7.01.03
MEM10K LIBRARY DATE:	05/15/87	MEM10K LIBRARY REVISION:	7.02.00

NETWORK STATISTICS AFTER CELL DELETIONS

NUMBER OF CELLS DELETED:	64
NUMBER OF UNCONNECTED CELL OUTPUTS:	1800
NUMBER OF INPUT PINS (EXCLUDING BIDIRECTIONAL PINS):	49
NUMBER OF OUTPUT PINS (EXCLUDING BIDIRECTIONAL PINS):	16
NUMBER OF BIDIRECTIONAL PINS:	68
TOTAL NUMBER OF I/O SIGNAL PINS USED:	133
RANGE OF POWER PINS REQUIRED (VSS & VDD) [min-max]:	20-40
NUMBER OF PAD LOCATIONS USED FOR INPUT PINS:	49
NUMBER OF PAD LOCATIONS USED FOR OUTPUT PINS:	16
NUMBER OF PAD LOCATIONS USED FOR BIDIRECTIONAL PINS:	68
TOTAL NUMBER OF PAD LOCATIONS USED FOR ABOVE:	133
TOTAL NUMBER OF UNRESERVED PAD LOCATIONS AVAILABLE:	211
NUMBER OF I/O DEVICE LOCATIONS USED FOR BUFFERS:	218
TOTAL NUMBER OF I/O DEVICE LOCATIONS AVAILABLE:	218

NUMBER OF CELLS USED:	5758	NUMBER OF GATES USED:	20553
NUMBER OF CELL TYPES:	103	ARRAY GATE USAGE (%):	40.38
MAXIMUM PINS PER NET:	318	~~ARRAY AREA USAGE (%):~~	~~40.82~~
NETS WITH 10<PINS/NET<=20:	83	NUMBER OF SIGNAL NETS:	5691
NETS WITH PINS/NET > 20:	62	AVERAGE PINS PER NET:	3.630

.BDCMD
.NET

10051

35% x 3.0/3.6 = 30%

32/33%

BUF8A

Philip Levin
BBN Advanced Computers Inc.
10 Fawcett Street
Cambridge, Ma. 02148

January 18, 1988

INTRODUCTION

I am currently designing a gate array with LSI using the LCA10075 compacted array. After conversations with my local Applications Engineer, I became concerned that my rather unusual clocking scheme may be difficult to handle in layout. This design presentation is aimed at informing the people most closely associated with the actual layout of my intentions. From this, I hope to anticipate any problems that I may encounter, so that I can make any necessary changes well before layout.

THE BASIC DESIGN

Figure 1 shows the basic block diagram of the design. Note that the four major blocks operate on separate clocks. These clocks are completely independent and are derived from separate pins. Synchronization between the blocks has been accounted for.

The latch shown Figure 1 represents approximately 50 latches that are used to increase hold time on the TBUS module (QH and QT have a defined phase relationship).

In the general, the design has the following characteristics:

- approximately 20,000 gates
- all random logic, no meagfunctions
- approximately 3.6 pins/net
- highly bus structured
- I/O intensive - all pins are used

IMPROVEMENTS FOR SPEED

Unfortunately, if the clock nets shown in Figure 1 were specified as clock nets and driven directly with a clock drivers, loading on those nets would force the "clock-to-Q" delay of the four modules to be unacceptably large. To get around this problem, I implemented the scheme shown in Figure 2.

Here, an external clock directly drives a set of "front-end" flip-flops to achieve the desired clock-to-Q delay. The "second-level" clock for each module is derived from that first level of drivers. Note that the CIO module does not have the clock-to-Q problem.

To reduce the number of specially handled clock nets, I have only specified the "second-level" nodes as clock nets (heavy lines). This should not pose a problem since first-level clocked elements do not "talk" to each other. In addition there should be no hold-time violation between second-level and first-level clocked elements because the second-level clock always lags the first-level clock (the DRV8I's are heavily loaded).

Therefore, I don't expect the timing alone will cause any problems, my concern is of course: layout.

PROPOSED LAYOUT

I have already used LPACE to group the top-level hierarchies (there are 18 of them) into three sections. This grouping should facilitate layout of the multi-clock scheme. Figure 3 shows some aspects of a proposed layout.

Note that the left half of the chip is devoted to the Tb clock net. I felt the best way to handle the other two clock nets, Rb and Sb, was to divide the chip into top and bottom halves as shown. I will ensure that the buffers will have the correct placement. In the .CFUN file, I will specify the three sections as "reigons" to prevent swapping cells out of their "clock-zone."

QUESTIONS

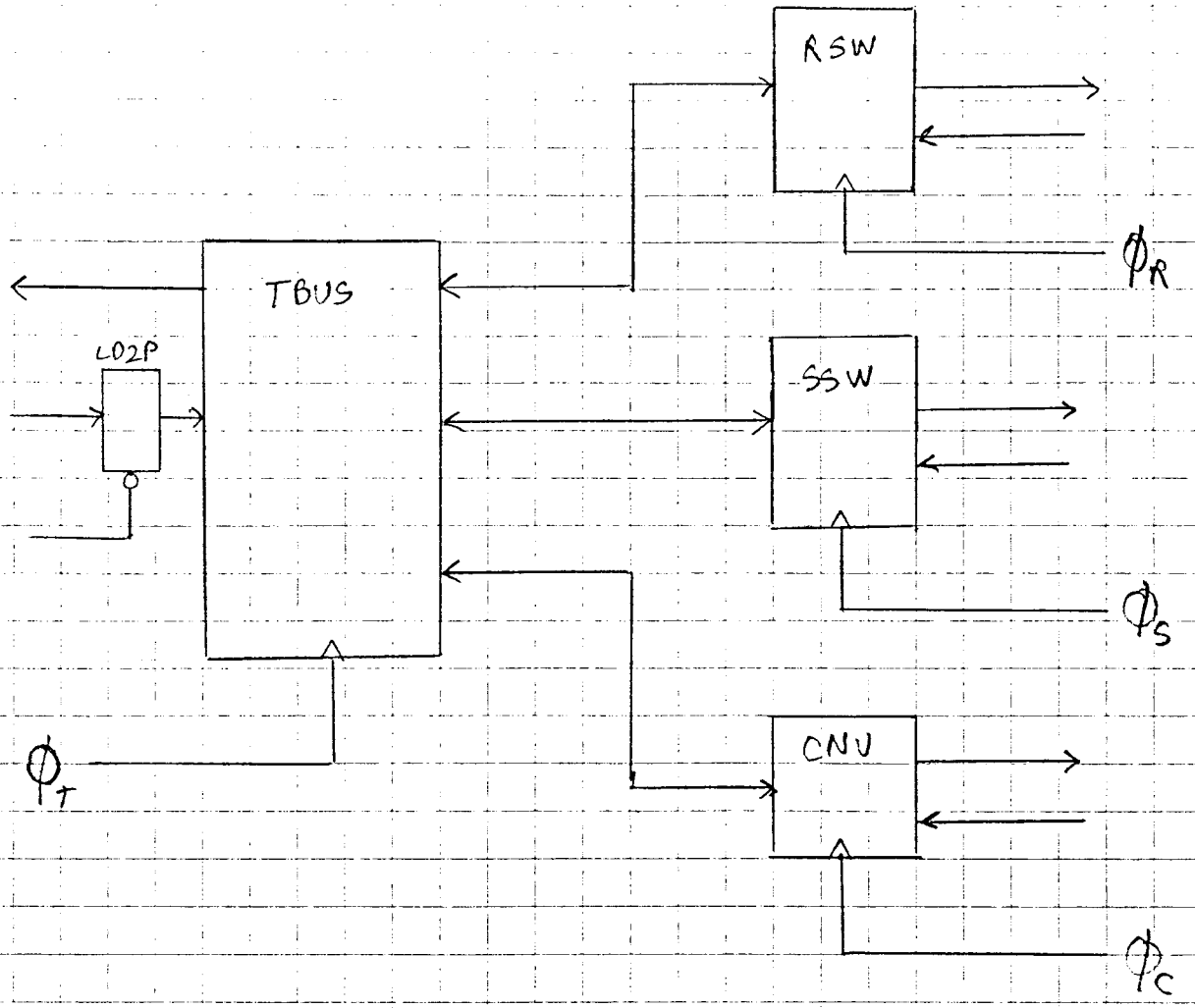
Besides the general question: "what do you think?" I have the following, more specific questions:

1) Will the "reigons" specification from LPACE be enough to prevent swapping out of the sections?

2) What will the max clock skew be between any two clocked elements in any of the three reigons?

3) Are there any recommendations for improvements?

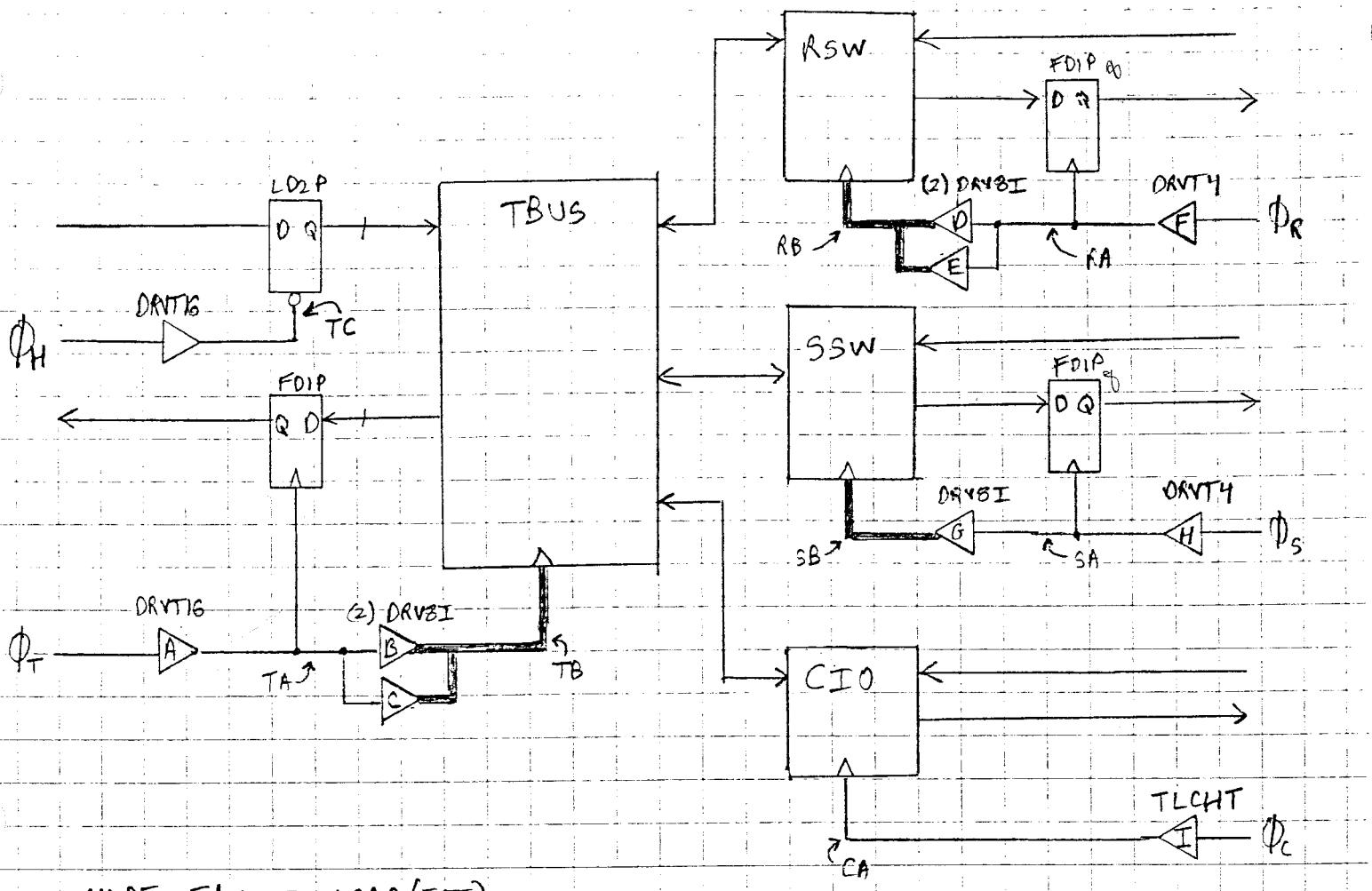
Phelps Lee



BLOCK DIAGRAM – CLOCKING SCHEME

FIGURE 1

1/8/87 CPL



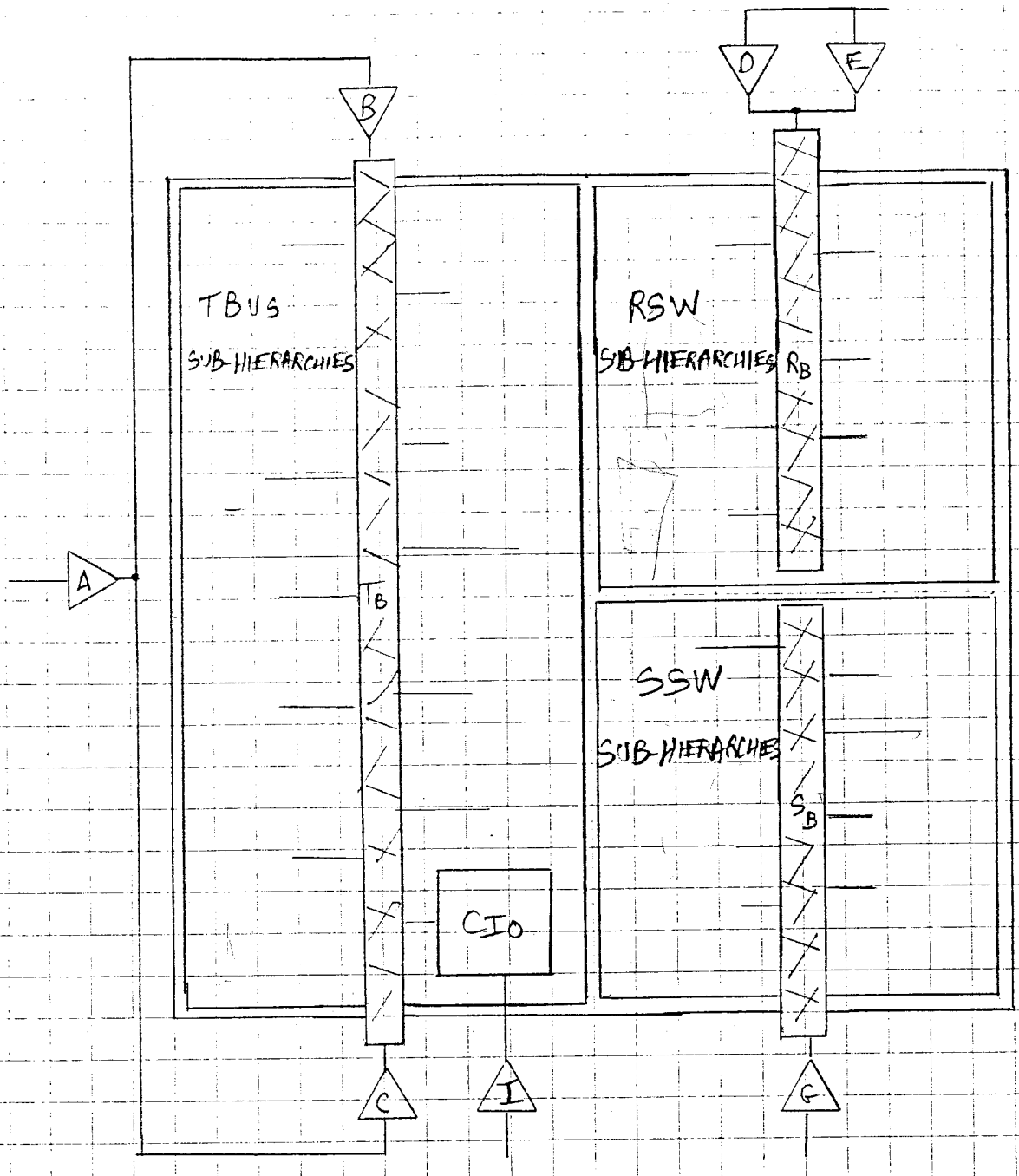
NODE	FANOUT	LOAD (EST.)
TA	115	350
TB*	220	—
TC	105	300
RA	25	80
RB*	210	—
SA	30	85
SB*	105	—
CA	15	40

*SPECIALLY TREATED CLOCK NETS (INDICATED ON SCHEMATIC WITH HEAVY LINES)

SCHEMATIC - CLOCKING SCHEME

FIGURE 2

1/8/88CPL



LAYOUT DIAGRAM - CLOCKING SCHEME

FIGURE 3

1/14/88 CPL

MARIA MICALAN

AMENDMENT

LISA SCHMERLING x4674

LSI Logic Corporation ("LSI") and Bolt, Beranek & Newman Inc ("BBN") entered into a LDS Software License Agreement dated June 25, 1987 (the "Agreement") which as amended provided BBN with a license to use two (2) copies of the Software (as that term is defined in the Agreement) for a period of one (1) year. This Agreement is modified as of _____ ____ , 1988 (herein the "Effective Date") as follows:

1. LSI hereby grants to BBN a fully paid license to use the Software (as defined in the Agreement) listed in Paragraph 4 below. In consideration for this grant the License Fees in Paragraph 4 below, less the license fees previously paid in the amount of seventy two thousand dollars ($72,000), shall become payable upon signature of this Amendment.

2. The term of this Amendment shall be for two years from the Effective Date unless sooner terminated in accordance with the terms and conditions of the Agreement and thereafter from year to year at the then current maintenance fees [redacted]

3. The Annual Maintenance Fee shown in Paragraph 4 below shall be payable annually in advance commencing on the Effective Date.

4. Schedule 1 of the Agreement is replaced by the following:

Software	# of Copies	License Fee	Maintenance Annual Fee
Silicon Integrator	1	$75,000	$13,500
LCA10000 Library	1	$30,000	$ 5,400

BBN agrees that its possession and use of the Software shall continue to be governed by all of the terms and conditions of the Agreement. Except as expressly modified above, the Agreement remains in full force and effect.

LSI LOGIC CORPORATION	BOLT, BERANEK & NEWMAN, INC.
By	By
Title	Title
Date	Date

HAMILTON AVNET
AND
LSI LOGIC CORPORATION
ASIC DESIGN TOOLS QUOTATION
PREPARED FOR
BOLT, BERANEK & NEWMAN, INC.

Quotation No. NEWF8-083
Date: November 8, 1988

ITEM	ORDER CODE	DESCRIPTION	LICENSE FEE	ANNUAL MAINTENANCE FEE
1	SW-S36-SLGR	Silicon Integrator	$75,000	$13,500
2	LL-S36-LCA1	LCA10000 Library	30,000	5,400
3	N.A.	Past License Fee Credit	($72,000)	N.A.
		Total	$33,000	$18,900

Notes:

1. This Quotation is valid for thirty days from the date above and is exclusive of any applicable taxes. FOB point is destination.
2. Software availability is five days after receipt of hard copy purchase order and signed software license.
3. Additional terms and conditions are defined in the MDE Software License Agreement included as part of this Quotation.

LSI LOGIC Corporation
1551 McCarthy Blvd
Milpitas CA 95035
408.433.3000
Telex 172.153
Fax 408.434.6422

CALLED DOUG PHIEL 11/9/88
WILL CALL BACK MID NXT WEEK

August 24, 1988

Mr. Dick Pado
BBN Delta Graphics
14100 S.E. 36th Street
Bellevue, WA 98006

Quote No. RH8084

Dear Mr. Pado:

LSI Logic is pleased to submit the following quotation for Silicon Integrator with the LMA9000 and LCA10000 Libraries. LSI Logic is able to offer a significant discount on nodes licensed at BBN in Bellevue by extending the license existing at BBN in Cambridge. This license extension discount is only possible if BBN uses a single point of contact with LSI Logic for all software issues. DISTRIBUTION.

A license extension is 20% of the original license and maintenance fees for the first 3 extra nodes. After the 4th node is licensed, the extension license drops to 10% of the original license fees. BBN in Cambridge has licensed the Silicon Integrator, LPACE, and the LCA10000 library. Each of these modules is available to BBN Bellevue at the 20% rate. The LMA9000 Library has not yet been licensed so the initial license needs to be purchased for that library. Should BBN decide to license both the LMA9000 and LCA10000 on all nodes, a multi-library credit would apply.

AS LSI Logic does OEM SUN Workstations a complete turnkey system may be purchased from LSI Logic. Pricing for the Sun workstations is attaches.

The Silicon Integrator consists of the following software modules:

Logic Simulation Package (LDS) provides the designer with graphic/ schematic netlist entry, compile, link, delay prediction, design verification, glitch detection, storage cell output checks, toggle coverage and tester interface checking and verification. The simulator provides three strength four state simulation with provisions for hierarchical design.

Logic Schematic Capture Package (LSED) provides the designer with single-key commands, hierarchical design support, automatic wiring, multiple windows, on-line error checking, boundless page, unlimited "zoom in" and "zoom out" capabilities and complex wire (bus and bundle) capability.

Logic Waveform Editor (LWAVE) provides the designer with graphics entry of user-generated waveform input patterns, powerful commands for editing waveforms and waveform groups, powerful bus editing facilities and graphically displayed simulation results which allow quick analysis of timing relationships.

Timing Analyzer (LCAP) enables the designer to identify and receive reports on critical paths in the circuit. Critical paths may include all paths, paths emanating from a single point or user defined paths.

Power Analyzer (LPOW) enables the designer to monitor power consumption (in milliwatts) the average power values (minimum and maximum) globally for the entire simulation and for intervals within the simulation where instantaneous power exceeds a peak threshold.

Logic Schematic Builder (LIBERATE) creates an LSED gate level schematic from a NDL ASCII netlist file. This package in conjunction with LSED will create a set of electrically correct schematics with busses and hierarchy. These schematics may then be modified with the LSI Logic graphics tools.

In addition to the Silicon Integrator package, the following options are available:

Floorplanner (LPACE) provides the designer with the ability to automatically place hierarchical logic blocks on a chip, obtain more accurate delay information, analyze the inter-block connectivity, change block aspect ratios, positions, or interconnection lengths to improve pre-layout estimated delays of the critical nets.

Using critical net information provided by the LDS delay predictor (LDEL) using RC-tree analysis, LPACE generates pop-up windows which list delay information pertaining to the specified nets.

Explanation: Floorplanning allows users to optimize performance when designing with LSI Logic's 1.5 micron HCMOS ASIC technology. Floorplanning is extremely useful when a designer plans to exercise the performance limits of the technology. Floorplanning will eliminate most performance surprises prior to layout consequently minimizing any possible delay during simulation and layout.

Important Note: The Floorplanning/Chip Planning software is required for designs over 10,000 used gates. Also a minimum of 24 MBytes main memory will be required to run this module.

Bonding Diagram (LBOND) enables the user to create a bonding diagram by defining the I/O connections between the package and the die. This program checks for mechanical and electrical rules violation and interactive error correction a special features of the software package.

Many of the above modules can be licensed independently. However, at least one module must be the Logic Simulation Package (LDS). LSI Logic is flexible in packaging the software per your requirements.

It is important to note that discounts on Non-Recurring Engineering (NRE) will be available to you if this software package is licensed.

If you have any questions regarding the software or quotation, please feel free to contact me at (408)433-7422.

Sincerely,

Rick Hyman
Regional Sales Manager
Software Products

RH:mj

Attachment

cc: Hans Schwarz, LSIL
Eric Fleischman, LSIL
Van Lewing, LSIL
Jim Bausano, LSIL
Mark Larsen, LSIL
Bill Fletcher, LSIL

PRICING: SUN 3 Workstation
CAMBRIDGE ONLY

Software Description	Order Code	3 Year License Fee	Annual Support Services
Base System			
o Silicon Integrator	SW-S36-SLGR	$75,000	$13,500
Silicon Libraries			
o LCA10000 Compacted Array	LL-S36-LCA1	30,000	5,400
o LMA9000 Micro Array	LL-S36-LMA9	20,000	3,600
o Multiple Library Credits *		(20,000)	
Base System Package Total:		$105,000	$22,500
Other Modules			
o LPACE/LBOND	LL-S36-FLPL	$ 15,000	$ 2,700

Additional Nodes:
- o For Nodes 2-4, the license fee is 20% of the above fees.
- o For Nodes 5 or greater, the license fee is 10% of the above fees.

Annual Support Service includes regular software updates and support through our Software Service Organization using a telephone "hotline".

See Notes

* Multple library credit applies if both the LCA1000 and LMA9000 are licensed on all 3 nodes.

BBN BELLEVUE LICENSE EXTENSION

PRICING: SUN 3 Workstation
CAMBRIDGE (ADD-ON)

Software Description	Order Code	3 Year License Fee	Annual Support Services
Base System			
o Silicon Integrator	SW-S36-SLGR	$15,000	$ 2,700
Silicon Libraries			
o LCA10000 Compacted Array	LL-S36-LCA1	6,000	1,080
o LMA9000 Micro Array	LL-S36-LMA9	20,000	~~3,600~~ 720
o Multiple Library Credits *		(20,000)	
Base System Package Total:		$ 21,000	$ 7,380
Other Modules			
o LPACE/LBOND	LL-S36-FLPL	$ 3,000	$ 540
o System Total without Library Credit		$44,000	$ 7,920
o System Total with Library Credit		$24,000	$ 7,920

Annual Support Service includes regular software updates and support through our Software Service Organization using a telephone "hotline".

See Notes

* Multple library credit applies if both the LCA1000 and LMA9000 are licensed on all 3 nodes.

BBN BELLEVUE LICENSE EXTENSION

PRICING: SUN 3 Workstation

Software Description	Order Code	3 Year License Fee	Annual Support Services
Base System			
o Silicon Integrator	SW-S36-SLGR	$15,000	$ 2,700
Silicon Libraries			
o LCA10000 Compacted Array	LL-S36-LCA1	6,000	1,080
o LMA9000 Micro Array	LL-S36-LMA9	20,000	3,600
o Multiple Library Credits *		(20,000)	
Base System Package Total:		$ 21,00	$ 7,380
Other Modules			
o LPACE/LBOND	LL-S36-FLPL	$ 3,000	$ 540
o System Total without Library Credit		$44,000	$ 7,920
o System Total with Library Credit		$24,000	$ 7,920

Annual Support Service includes regular software updates and support through our Software Service Organization using a telephone "hotline".

See Notes

* Multple library credit applies if both the LCA1000 and LMA9000 are licensed on all 3 nodes.

SUN Hardware Pricing

Order Code	Description	Price
HW-S99-360FC16P14	o SUN 3/60FC-16-P14 Color Workstation (3 MIPS) Includes: - 16 MBytes Main Memory - 327 MBytes Disk - 60 MByte inch tape drive	$29,300/ea
MT-S99-HWMT	Support	$3,480/yr
HW-S99-SYS301	O/S Manuals	$ 550
IN-999-INSL	Installation	$ 2,000
	Availability	Call for Availability
HW-S993260P15	SUN 3/260 C-P15 Color Workstation (4 MIPS) Includes: - 8 MBytes Main Memory - 654 MByte Disk - 60 MByte 1/4 inch tape drive	$52,500/ea
MT-S99-HWMT	Support	$ 6,600/yr
HW-S99-SYS301	O/S Manuals	550
IN-999-INSL	Installation	$ 2,000
	Availability	30 days
HW-S99-108A	o 8MByte Expansion Board for 3/260	$ 8,000
MT-S99-HWMT	o Annual Maintenance for for 8MByte Board	$ 240

NOTES:

1. The software modules or package must be licensed for each node requiring a technology/silicon library.

2. All prices in this quotation are exclusive of any applicable software and hardware taxes.

3. This quotation is valid for 30 days from the above date.

Hamilton Avnet ELECTRONICS
AN AVNET COMPANY
10 D Centennial Drive ☐ Peabody, Massachusetts 01960 (617) 532-3701

July 12, 1988

Bolt, Beranek and Newman
10 Fawcett Street
Cambridge, Ma. 02238

Attn: Robert Stone

Dear Bob,

Hamilton/Avnet and LSI Logic are pleased to offer the following quotation for the LSI Logic ASIC design and analysis toolset. This quotation is for a two year license that will require only an annual maintenance fee to remain at the proper revision level. In the quotation you will notice that a full credit has been applied for the program license fee BBN has already purchased. Currently BBN is operating under a "no charge" license extention that is in effect through 9/25/88. The two year license purchase will require the attached amendment to be signed and returned to LSI logic. If you have any questions please call me at 596-7829.

Regards,

JOHN WONG

Mark A. Trulli
Technical Sales Manager
Hamilton/Avnet Electronics

CC:
	John Goodhue	BBN
	Phil Levin	BBN
	Rupert Stanley	H/A
	Jim Pena	LSIL
	Bill Fletcher	LSIL

HAMILTON/AVNET
AND
LSI LOGIC CORPORATION
ASIC DESIGN TOOLS QUOTATION
PREPARED FOR
BOLT, BERANEK & NEWMAN, INC.

Quotation No. NEWF8-037
Date: July 5, 1988

ITEM	ORDER CODE	DESCRIPTION	LICENSE FEE	ANNUAL MAINTENANCE FEE
1	SW-S36-SLGR	Silicon Integrator LSED, LWAVE, LCAP, LPOW, LOC CORE	$75,000	$13,500
2	SW-S36-SLGR	Silicon Integrator Additional Node	$15,000	$ 2,700
3	SW-S36-FLPL	Floorplanner - LPACE, LBOND	$15,000	$ 2,700
4	LL-S36-LCA1	LCA10000 Library	$30,000	$ 5,400
5	LL-S36-LCA1	LCA10000 Library Additional Node	$ 6,000 141,000	$ 1,080
6	N.A.	Past License Fee Credit	($72,000)	N.A.
		Total	$69,000	$25,380

Notes:

1. This Quotation is valid for sixty days from the date above and is exclusive of any applicable taxes. FOB point of destination.

2. Software availability is five days after receipt of hard copy purchase order and signed software license.

3. Additional terms and conditions are defined in the MDE Software License Agreement included as part of this Quotation.

- STATE MACHINE
- LOGIC SYNTHESIS TOOL BY INTERNALLY DEVELOPMENT

AMENDMENT

LSI LOGIC CORPORATION ("LSI") and BOLT, BERANEK & NEWMAN, INC. ("BBN") entered into a LDS Software License Agreement dated June 25, 1987 (the "Agreement") which as amended provided BBN with a license to use two (2) copies of the Software (as that term is defined in the Agreement) for a period of one (1) year. This Agreement is modified as of June 25, 1988 (herein the "Effective Date") as follows:

1. LSI hereby grants to BBN a fully paid license to use the Software (as defined in the Agreement) listed in Paragraph 4 below. In consideration for this grant the License Fees in Paragraph 4 below, less the license fees previously paid in the amount of Seventy-Two Thousand Dollars ($72,000), shall become payable upon signature of this Amendment.

2. The term of this Amendment shall be for two years from the Effective Date unless sooner terminated in accordance with the terms and conditions of the Agreement and thereafter from year to year at the then current maintenance fees provided the Software is being made available by LSI to the general marketplace.

3. The annual maintenance fee show in Paragraph 4 below shall be payable annually in advance commencing on the Effective Date.

Software	# of Copies	License Fee	Maintenance Annual Fee
Silicon Integrator	2	$90,000	$16,200
Floorplanner	1	15,000	2,700
LCA10000 Library	2	36,000	6,480

BBN agrees that its possession and use of the Software shall continue to be governed by all of the terms and conditions of the Agreement. Except as expressly modified above, the Agreement remains in full force and effect.

LSI LOGIC CORPORATION

By_____

Title_____

Date_____

BOLT, BERANEK & NEWMAN, INC.

By_____

Title_____

Date_____

AMENDMENT

LSI LOGIC CORPORATION ("LSI") and BOLT, BERANEK & NEWMAN, INC. ("BBN") entered into a LDS Software License Agreement dated June 25, 1987 (the "Agreement") which as amended provided BBN with a license to use two (2) copies of the Software (as that term is defined in the Agreement) for a period of one (1) year. This Agreement is modified as of June 25, 1988 (herein the "Effective Date") as follows:

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LCA10000 Library	2	36,000	6,480

BBN agrees that its possession and use of the Software shall continue to be governed by all of the terms and conditions of the Agreement. Except as expressly modified above, the Agreement remains in full force and effect.

LSI LOGIC CORPORATION

By_____

Title_____

Date_____

BOLT, BERANEK & NEWMAN, INC.

By_____

Title_____

Date_____

REQUISITION

148132

RECEIVED JUN 4 1987

INSTRUCTIONS

1. COMPLETE ALL APPLICABLE UNSHADED BOXES.
2. DO NOT WRITE IN SHADED BOXES.
3. REQUISITIONER – RETAIN LAST COPY.
4. FORWARD TO NEXT HIGHEST APPROVAL REQUIRED.

REQUISITION DATE: 22 (Day) 5 (Month) 87 (Year)	REQUISITIONER: Philip Levin	CHECK ONE: ☑ ORIGINAL REQUEST ☐ CHANGE TO P.O. NO. ☐ BLANKET P.O. NO.	BUYER NO. / CONFIRMING: ☐ YES ☐ NO
DEPT. NO.: 0 1 0	JOB NO.: 1 3 1 8 3 0	ACCOUNT NO.: 5TO 29	PURCHASE ORDER NO.: 72433 / CHANGE
GOVERNMENT CONTRACT NO.: —	GOVT. PRIORITY: —	GOVERNMENT PROPERTY: ☐ CONTROLLABLE ☐ EXPENDABLE ☐ DELIVERABLE	
PCO: ☐ ADVANCE NOTIFICATION REQUIRED ☐ WRITTEN CONSENT REQUIRED	ACO: ☐ ADVANCE NOTIFICATION REQUIRED ☐ WRITTEN CONSENT REQUIRED	DATE ORDER PLACED (Day / Month / Year)	BUYER INIT.
INTERNAL DESTINATION: 11/446 (Location) P. Levin (Person)	SHIP TO: ☐ 87 FAWCETT STREET, CAMBRIDGE, MA 02238 ☒ OTHER: 10 Fawcett Street	TAXABLE: ☐ YES ☐ NO	COMPETITION CODE
F.O.B.	SHIP VIA	SHIPMENT TERMS: ☐ PREPAID ☐ COLLECT	PAYMENT TERMS: N30 / SUPPLIER NO.

SUGGESTED SUPPLIER

LSI LOGIC

1601 Trapelo Road

Waltham, MA 02154

Jim Pena —

SELECTED SUPPLIER

LSI Logic

ATTN: Jim Pena

ITEM	QUANTITY	U/M	DESCRIPTION	DELIVERY REQUIRED (Day / Mo. / Year)	ESTIMATED PRICE	UNIT PRICE	AMOUNT
1			Non recurring engineering for LCA10051 compacted gate array (Level IIB interface)		89,500		
2			Program License fee for two nodes (Sur. Workstations)		60,000		
				EST. TOTAL ▶	$149,500	TOTAL ▶	

UNIT OF MEASURE CODE: BX-Box, C-Hundred, CS-Case, CT-Carton, CY-Cylinder, DA-Day, DR-Drum, DZ-Dozen, EA-Each, FT-Foot, G-Gram, GL-Gallon, GR-Gross, KG-Kilogram, L-Litre, LB-Pound, LT-Lot, M-Thousand, ME-Meter, MO-Month, OZ-Ounce, PR-Pair, PT-Pint, QT-Quart, RL-Roll, ST-Set, TO-Troy Ounce, YD-Yard

REMARKS (Requisitioner to Buyer)

Item 1 & 2 are per LSI quote

Final quote to follow

APPROVAL SIGNATURES

REQUISITIONER	DATE	NAME	DATE
Philip Levin	5/27/87	Paul Carter	6/4/87
NAME	DATE	NAME	DATE
[illegible]	5/27/87	N. Mathis	6/3/87
NAME	DATE	NAME	DATE
[illegible]	5/29/87		
NAME	DATE	NAME	DATE
Michael S. Jones			

REMARKS (Buyer to Supplier)

LSI LOGIC CORPORATION
AND
HAMILTON/AVNET
SOFTWARE QUOTATION
FOR
BBN - ADVANCED COMPUTER, INC.

OLD QUOTE

MULTIPLE COPY LICENSE PROPOSAL

Date: April 27, 1987
Quote Number: NEWG87-033

SOFTWARE FOR SUN MICROSYSTEMS WORKSTATION	LICENSE FEE	ANNUAL MAINTENANCE
LDS III		
Initial multicopy license and first node fee	$65,000	$11,700

3 year license to run LDS simulator software on SUN Microsystems workstations running the Unix 4.2bsd operating system.

This license gives the user the ability to do network capture, functional simulation, timing simulation and test extraction. Specifically, this system consists of the following modules:

- Netlist Capture
- Compile (LCMP)
- Link (LLINK)
- Delay Generator (LDEL)
- Single Chip Simulator (LSIM)
- Test Vector Extraction (LTEST)
- Verify (LVER)

LDS GRAPHICS MODULE		
Initial multicopy license and first node fee	$15,000	$2,700

LDS Graphics gives the user the ability to graphically capture schematics and generate net lists. It also features an advanced graphics based wave form simulation set-up and display.

MULTIPLE COPY LICENSE PROPOSAL (CONT.)

Date: April 27, 1987
Quote Number: NEWG87-033

	LICENSE FEE	ANNUAL MAINTENANCE
LDS LIBRARY		
Initial multicopy license and first node fee		
3 year license to use the LDS library with the LDS simulator on a SUN Microsystems workstations.		
LCA10000 Series Compacted Array Macrocell Function and Performance Libraries.	$80,000	$14,400
MEGALCA Series Compacted Array Megafunction Library.	$50,000	$9,000
SOFTWARE INSTALLATION		
Installation and training for LDS-III on a SUN workstation.	$5,000	

The license fee totals $210,000. In recognition of the potential value of the long term relationship, we are offering this package for a license fee of $180,000. Annual maintenance is $37,800.

ADDITIONAL NODES

1. This license would grant BBN-ADVANCED COMPUTER, INC., the right to install the LDS Software and technology libraries on up to five (5) SUN workstations nodes at this site. An additional per copy fee and annual maintenance fee associated with each multiple node follows. The price for the first node is included in the initial license fee.

	LICENSE FEE	ANNUAL MAINTENANCE
2nd through 5th	$42,000	$2,000

Date: April 27, 1987
Quote Number: NEWG87-033

2. This maintenance plan requires that BBN-ADVANCED COMPUTER, INC., set up an internal support group to act as the point of contact for software updates and problems or questions.

SHORT TERM RENTAL

The fee for a three month rental of this software is $50,000 for the first copy and $10,000 for a second copy. This includes installation and maintenance. We will apply the rental fee to a fully license if the conversion is done during the rental period.

OLD QUOTE

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

I. PRODUCT PROPOSED

In response to your RFQ Hamilton/Avnet proposed the following device:

CUSTOMER DESCRIPTION	LSI LOGIC DEVICE	TOTAL GATES	EST. USABLE GATES	PACKAGE TYPE
RFQ	LCA10100	100,182	40,000	223 CPGA
RFQ	LCA10051	50,904	20,000	155 CPGA

II. NON-RECURRING ENGINEERING (NRE) PRICING

LSI LOGIC DEVICE	INTERFACE	TOTAL ($)
LCA10100	IIB	$134.K
LCA10051	IIB	$89.5K
LCA10100	IIA	$240.5K
LCA10051	IIA	$168.5K

The Division of responsibility between BBN and Hamilton-Avnet for a IIB interface per LSI statement of work (attachment A of H/A contract).

A. Included in the NRE price is delivery of 10 prototypes per device. These prototypes are electrically tested only; no environmental or reliability testing of the prototypes will be performed.

B. A one week design class is included with a Level II interface.

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

C. PAYMENT SCHEDULE

H/A will invoice in accordance with the following schedule:

CUSTOMER DESCRIPTION	LSI LOGIC DEVICE	1NRE -ASS	2NRE -ASC	3NRE -APG	4NRE -ADP	TOTAL NRE
RFQ	LCAXXXXX	20%	20%	40%	20%	100%

LINE TYPES:

1NRE-ASS = At start of simulation at LSI LOGIC .

2NRE-ASC = At simulation completion.

3NRE-APG = At PG TAPE generation.

4NRE-ADP = At delivery of prototypes.

PRT_PROTOTYPES = 10 prototype units included in NRE price.

III. PRODUCTION PRICING

LSI LOGIC DEVICE	PKG TYPE	YEAR	1K	5K	10K
LCA10100	223 CPGA	1988	$311.40	$206.33	$193.77
LCA10051	155 CPGA	1988	$166.79	$110.51	$103.84
MINIMUM SHIPMENT QUANTITY			250	1000	2.5K

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

THIS PRICING ASSUMES:

1. Processing: STANDARD COMMERCIAL (0 C to 70 C , VCC ±5%)

2. Minimum order guidelines: Sixty (60) day maximum between first and last requested delivery on purchase order.

- $7,500. COMMERCIAL

- If sufficient die in stock to cover assembly run, the minimum order would be: $5,500. COMMERCIAL

- $2,500. minimum on orders from box stock. Under $2.5k OK if order depletes existing stock.

IV. NON-RECURRING ENGINERRING SCHEDULE

Schedules provided are approximate and are to be used for planning purposes only.

STEP	TIME FROM PREVIOUS STEP
1NRE-ASS	*
2NRE-ASC	*
LAYOUT	1 WEEK/10K GATES
3NRE-APG	*
4NRE-ADP	6

* BOTH SIMCPL AND SIMAPG ARE CUSTOMER CONTROLLED.

V. PRODUCTION SCHEDULE

12 weeks ARO

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

VI. DESIGN INTERFACE

LEVEL	DESCRIPTION
IIA	All design work done at LSI Logic Design Center
IIB	Design work done at customer site using LDS III
IIC	Schematic capture done at customer site with SOFTWARE DATA BOOK
IID	Preliminary design work done at customer site with DESIGN VERIFIER
III	TURNKEY design with schematics, critical timing and test vectors from customer

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

I. PRODUCT PROPOSED

In response to your RFQ Hamilton/Avnet proposed the following device:

CUSTOMER DESCRIPTION	LSI LOGIC DEVICE	TOTAL GATES	EST. USABLE GATES	PACKAGE TYPE
RFQ	LCA10100	100,182	40,000	223 CPGA
RFQ	LCA10075	74,970	30,000	155 CPGA
RFQ	LCA10051	50,904	20,000	155 CPGA
RFQ	LCA10038	37,932	15,000	155 CPGA

II. NON-RECURRING ENGINEERING (NRE) PRICING

LSI LOGIC DEVICE	IIB INTERFACE	IIA INTERFACE
LCA10100	$134.K	$240.5K
LCA10075	$113.5K	$207.K
LCA10051	$89.5K	$168.5K
LCA10038	$74.5K	$130.K

The Division of responsibility between BBN and Hamilton-Avnet for a IIB interface per LSI statement of work (attachment A of H/A contract).

A. Included in the NRE price is delivery of 10 prototypes per device. These prototypes are electrically tested only; no environmental or reliability testing of the prototypes will be performed.

B. A one week design class is included with a Level II interface.

Hamilton Avnet ELECTRONICS
AN AVNET COMPANY

10 D Centennial Drive ☐ Peabody, Massachusetts 01960 (617) 532-3701

BBN-ACI
10 Faucet St.
Cambridge, MA 02238

April 26, 1987

ATTENTION : Ward Hariman
SUBJECT: Gate Array QUOTATION

DEAR Ward,

Hamilton/Avnet Electronics and LSI Logic are pleased to offer a custom HCMOS design program in response to your requirements.

Quote #DE487-58 has been assigned to this quotation. Please reference this number in all future correspondence. This quotation is valid for thirty (30) days.

Hamilton/Avnet looks foreward to a mutually successful business relationship with you. Should you have any futher questions or if I can be of help in any way, please do not hesitate to call me.

Sincerely,

Mark A. Trulli
ASIC Specialist
Hamilton/Avnet Electronics

cc: Randy Rettberg, BBN-ACI
Phil Levin, BBN-ACI
Arthur Babitz, BBN-ACI
Lynne Roberts, H/A
Rupert Stanley,H/A
Jim Pena, LSIL

BBN ADVANCED COMPUTER INC.
10 FAWCETT STREET
CAMBRIDGE MA 02238

TELEPHONE: 617-491-1850

Send Invoice in Triplicate to:
Accounts Payable Dept.
10 Moulton Street
Cambridge, MA 02238

This Number must appear on ALL packages shipping papers, invoices and correspondence.

PURCHASE ORDER
ORDER NO. 77127

SHIP TO: 87 FAWCETT ST., CAMBRIDGE, MA 022.
UNLESS NOTED BELOW:

(*3758*)

TO
LSI LOGIC
C/O HAMILTON AVNET
ASIC DEPT.
10 D CENTENNIAL DRIVE
PEABODY MA 01960
ATTENTION: Rupert Stanley

ORDER DATE	DELIVERY REQUIRED	TAXABLE	RESALE PERMIT NO.	SHIP VIA	F.O.B.	TERMS
23Dec87	28Dec87	YES ___ NO X	042-164-398	Fed X	SP	Net 30

REQUISITIONER	REQUISITION NO.	JOB NO.	ACCOUNT NO.	DEPT.	GOVERNMENT CONTRACT NO.	GOVT. PRIORITY
P. Levin	153835	131830	4001-10-131830	10		

BBN Ref. 7607 GP:

ITEM	QUANTITY	U/M	DESCRIPTION	UNIT PRICE	AMOUNT
1	1.00	ea	SW-509-CRIT Timing Analyzer (LCAP)	12000.0000	$12000.00
2	1.00	ea	MT-509-CRIT Maintenance for LCAP	0.0000	$0.00

Terms and Conditions:
BBN Agrees that the LCAP module will be governed by the terms and conditions of the software license agreement between LSI Logic and Bolt Beranek and Newman Inc. dated 25 JUN 87. The license remains in full force and effect.

IT	BX - Box	CY - Cylinder	EA - Each	GR - Gross	LT - Lot	OZ - Ounce	RL - Roll
RE	C - Hundred	DA - Day	FT - Foot	KG - Kilogram	M - Thousand	PR - Pair	ST - Set
JE	CS - Case	DR - Drum	G - Gram	L - Litre	ME - Meter	PT - Pint	TO - Troy Ounce
	CT - Carton	DZ - Dozen	GL - Gallon	LB - Pound	MO - Month	QT - Quart	YD - Yard

CURRENT P.O. VALUE

UBSTITUTIONS PERMITTED
SS AUTHORIZED BY BUYER

BUYER: P. STONE
TEL. NO.: 497 – 3609
BUYER'S SIGNATURE

$12000.00

REQUISITIONER

BBN ADVANCED COMPUTER INC.
10 FAWCETT STREET
CAMBRIDGE MA 02238

TELEPHONE: 617-491-1850

Send Invoice in Triplicate to:
Accounts Payable Dept.
10 Moulton Street
Cambridge, MA 02238

This Number must appear on ALL packages shipping papers, invoices and correspondence.

PURCHASE ORDER

ORDER NO.	CHG.
77126	0

(*3758*)

TO
LSI LOGIC
C/O HAMILTON AVNET
ASIC DEPT.
10 D CENTENNIAL DRIVE
PEABODY MA 01960
ATTENTION: Rupert Stanley

SHIP TO: 87 FAWCETT ST., CAMBRIDGE, MA 02238
UNLESS NOTED BELOW:

ORDER DATE	DELIVERY REQUIRED	TAXABLE	RESALE PERMIT NO.	SHIP VIA	F.O.B.	TERMS
23Dec87	15Mar88	YES ___ NO X	042-164-398	FED X	SP	Net 30

REQUISITIONER	REQUISITION NO.	JOB NO.	ACCOUNT NO.	DEPT.	GOVERNMENT CONTRACT NO.	GOVT. PRIORITY
P. Levin	148132	131830	5029-10-131830	10		

BBN Ref. 7607 GP:

ITEM	QUANTITY	U/M	DESCRIPTION	UNIT PRICE	AMOUNT
1	1.00	lt	BBN SIGA Non Recurring engineering cost for LCA10051 compacted gate array (Level II b interface) including 10 prototypes. Terms and Conditions: This Agreement shall be in accordance with Quote DE487-58 and BBN's Agreement for Custom Product Development to be negotiated as mutually acceptable.	89500.0000	$89500.00

UNIT OF MEASURE CODE

BX - Box	CY - Cylinder	EA - Each	GR - Gross	LT - Lot	OZ - Ounce	RL - Roll
C - Hundred	DA - Day	FT - Foot	KG - Kilogram	M - Thousand	PR - Pair	ST - Set
CS - Case	DR - Drum	G - Gram	L - Litre	ME - Meter	PT - Pint	TO - Troy Ounce
CT - Carton	DZ - Dozen	GL - Gallon	LB - Pound	MO - Month	QT - Quart	YD - Yard

CURRENT P.O. VALUE

NO SUBSTITUTIONS PERMITTED UNLESS AUTHORIZED BY BUYER

BUYER	TEL. NO.	BUYER'S SIGNATURE
R. STONE	497 - 3609	

$89500.00

REQUISITIONER

INSTRUCTIONS

1. COMPLETE ALL APPLICABLE UNSHADED BOXES.
2. DO NOT WRITE IN SHADED BOXES.
3. REQUISITIONER – RETAIN LAST COPY.
4. FORWARD TO NEXT HIGHEST APPROVAL REQUIRED.

REQUISITION

144669

REQUISITION DATE (Day / Month / Year)	REQUISITIONER	CHECK ONE: ☐ ORIGINAL REQUEST ☐ CHANGE TO P.O. NO. ____ ☐ BLANKET P.O. NO. ____		BUYER NO.	CONFIRMING ☐ YES ☐ NO
DEPT. NO.	JOB NO.	ACCOUNT NO.		PURCHASE ORDER NO.	CHANGE
GOVERNMENT CONTRACT NO.		GOVT. PRIORITY	GOVERNMENT PROPERTY ☐ CONTROLLABLE ☐ EXPENDABLE ☐ DELIVERABLE		
PCO ☐ ADVANCE NOTIFICATION REQUIRED ☐ WRITTEN CONSENT REQUIRED		ACO ☐ ADVANCE NOTIFICATION REQUIRED ☐ WRITTEN CONSENT REQUIRED		DATE ORDER PLACED (Day / Month / Year)	BUYER INIT.
INTERNAL DESTINATION (Location / Person)	SHIP TO ☐ 87 FAWCETT STREET, CAMBRIDGE, MA 02238 ☐ OTHER:			TAXABLE ☐ YES ☐ NO	COMPETITION CODE
F.O.B.	SHIP VIA	SHIPMENT TERMS ☐ PREPAID ☐ COLLECT	PAYMENT TERMS	SUPPLIER NO.	
SUGGESTED SUPPLIER		SELECTED SUPPLIER			

ITEM	QUANTITY	U/M	DESCRIPTION	DELIVERY REQUIRED (Day / Mo. / Year)	ESTIMATED PRICE	UNIT PRICE	AMOUNT

UNIT OF MEASURE CODE: BX-Box, C-Hundred, CS-Case, CT-Carton, CY-Cylinder, DA-Day, DR-Drum, DZ-Dozen, EA-Each, FT-Foot, G-Gram, GL-Gallon, GR-Gross, KG-Kilogram, L-Litre, LB-Pound, LT-Lot, M-Thousand, ME-Meter, MO-Month, OZ-Ounce, PR-Pair, PT-Pint, QT-Quart, RL-Roll, ST-Set, TO-Troy Ounce, YD-Yard

EST. TOTAL ▶ | TOTAL ▶

REMARKS (Requisitioner to Buyer)	APPROVAL SIGNATURES				REMARKS (Buyer to Supplier)
	REQUISITIONER	DATE	NAME	DATE	
	NAME	DATE	NAME	DATE	
	NAME	DATE	NAME	DATE	
	NAME	DATE	NAME	DATE	

REQUISITIONER

BLD. 1 50 MOULTON

1067

CHRIS McMAHON

Hamilton Avnet ELECTRONICS
AN AVNET COMPANY
10 D Centennial Drive ☐ Peabody, Massachusetts 01960 (617) 532-3701

June 8, 1988

BBN Corp
87 Fawcett Street
Cambridge, MA 02238

Attention: Vince Santarlasci

Dear Vince,

This quotation is for the LSI Logic LCA10051 device that is being designed by BBN-ACI. I have included pricing for the following items:

1. Hot Lot Prototype Processing
2. Additional Prototypes
3. Preproduction Unit Pricing

1. Hot Lot Prototype processing is an expedite service available to customers in need of a "Faster" prototype turnaround. The process needs to be initiated by a purchase order before AC sign off of the device. The normal LSI Logic prototype lead-time is 5 weeks from AC sign off. Expedite fee's are as follows:

   4 week Turnaround = $10.K
   3 week Turnaround = $20.K
   2 week Turnaround = $30.K

2. Additional prototype units:

Device	1 - 50	Delivery
LCA10051 155 CPGA	$537.08	6 wks. ARO

3. Preproduction units are available provided BBN places the order prior to AC sign off of the design. The unit price is invoiced in two Line items. "RSK" represents 60% of the total unit price and a $2500 Lot start charge amortized over the total number of units ordered. This Line item is invoiced at waffer start. "PRE" represents 40% off the total unit price and is invoiced at delivery of the preproduction units. Delivery of the preproduction units is 8-10 weeks ARO.

	100	250	500	LSI LOGIC DEVICE
RSK	$186.12	$110.07	$ 93.19	LCA10051
PRE	$107.42	$ 66.72	$ 58.79	155 CPGA
TOTAL	$293.54	$176.79	$151.98	

Hamilton/Avnet ELECTRONICS
AN AVNET COMPANY

10 D Centennial Drive ☐ Peabody, Massachusetts 01960 (617) 532-3701

If you have any questions please call me at 596-7829.

Regards,

Mark A. Trulli

cc: John Goodhue, BBN
Phil Levin, BBN
Jim Pena, LSI
Rupert Stanley, H/A

Hamilton Avnet ELECTRONICS
AN AVNET COMPANY
10 D Centennial Drive ☐ Peabody, Massachusetts 01960 (617) 532-3701

June 8, 1988

BBN Corp
87 Fawcett Street
Cambridge, MA 02238

Attention: Vince Santarlasci

Dear Vince,

The following quotation is for the Fault Grading Services from LSI Logic Corp. The prices have been generated for the LCA 10051 (SIGA Array) being designed by ACI. LSI Logic offers two methods of fault grading that you may choose to initiate. Exhaustive analysis fault grading is a "full" comprehensive test yielding highly accurate results. Statistical analysis fault grading is a lower cost alternative to the exhaustive method and yields results that have a +3% confidence when compared to exhaustive method results. Please refer to the attached document "LDS Fault Grading" for a complete description of the Fault grading procedure.

The Fault grading charges take the form of a Base Run and Additional Runs. BBN may elect to run several additional runs in which the test vectors are enhanced to increase coverage. Test vectors may be added in 4000 vector blocks for the additional runs.

STATISTICAL ANALYSIS

Base Run: $13.1K
Each Additional Run: $1.9K
Lead time from submission of test to results: 1 wk.

EXHAUSTIVE ANALYSIS

Base Run: $57.K
Each Additional Run: $8.2K
Lead time from submission of test to results: 2-3 wks.

If you have any questions please call me at 596-7829.

Regards,

Mark A. Trulli

cc: John Goodhue, BBN
Phil Levin, BBN
Jim Pena, LSI
Rupert Stanley, H/A

Hamilton/Avnet ELECTRONICS
An AVNET COMPANY

10 D Centennial Drive ☐ Peabody, Massachusetts 01960 (617) 532-3701

BBN-ACI
10 Fawcet St.
Cambridge, MA 02238

May 20, 1987

ATTENTION : Ward Hariman
SUBJECT: Gate Array QUOTATION

DEAR Ward,

Hamilton/Avnet Electronics and LSI Logic are pleased to offer a custom HCMOS design program in response to your requirements.

Quote #DE487-58 has been assigned to this quotation. Please reference this number in all future correspondence. This quotation is valid for thirty (30) days.

Hamilton/Avnet looks foreward to a mutually successful business relationship with you. Should you have any futher questions or if I can be of help in any way, please do not hesitate to call me.

Sincerely,

Mark A. Trulli
ASIC Specialist
Hamilton/Avnet Electronics

cc: Randy Rettberg, BBN-ACI
Phil Levin, BBN-ACI
Arthur Babitz, BBN-ACI
Lynne Roberts, H/A
Rupert Stanley,H/A
Jim Pena, LSIL

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

I. PRODUCT PROPOSED

In response to your RFQ Hamilton/Avnet proposed the following device:

CUSTOMER DESCRIPTION	LSI LOGIC DEVICE	TOTAL GATES	EST. USABLE GATES	PACKAGE TYPE
RFQ	LCA10100	100,182	40,000	223 CPGA
RFQ	LCA10051	50,904	20,000	155 CPGA

II. NON-RECURRING ENGINEERING (NRE) PRICING

LSI LOGIC DEVICE	INTERFACE	TOTAL ($)
LCA10100	IIB	$134.K
LCA10051	IIB	$89.5K
LCA10100	IIA	$240.5K
LCA10051	IIA	$168.5K
LCA100 [illegible]	2B	$174.5K
LCA100 75	2B	$ 113.5K

The Division of responsibility between BBN and Hamilton-Avnet for a IIB interface per LSI statement of work (attachment A of H/A contract).

A. Included in the NRE price is delivery of 10 prototypes per device. These prototypes are electrically tested only; no environmental or reliability testing of the prototypes will be performed.

B. A one week design class is included with a Level II interface.

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

C. PAYMENT SCHEDULE

H/A will invoice in accordance with the following schedule:

CUSTOMER DESCRIPTION	LSI LOGIC DEVICE	1NRE -ASS	2NRE -ASC	3NRE -APG	4NRE -ADP	TOTAL NRE
RFQ	LCAXXXXX	20%	20%	40%	20%	100%

LINE TYPES:

1NRE-ASS = At start of simulation at LSI LOGIC .

2NRE-ASC = At simulation completion.

3NRE-APG = At PG TAPE generation.

4NRE-ADP = At delivery of prototypes.

PRT_PROTOTYPES = 10 prototype units included in NRE price.

III. PRODUCTION PRICING

LSI LOGIC DEVICE	PKG TYPE	YEAR	1K	5K	10K
LCA10100	223 CPGA	1988	$311.40	$206.33	$193.77
LCA10051	155 CPGA	1988	$166.79	$110.51	$103.84
MINIMUM SHIPMENT QUANTITY			250	1000	2.5K
LCA038	155 CPGA			$ 94.14	
LCA075	155 CPGA			$ 151.55	

HAMILTON/AVNET
AND
LSI LOGIC
QUOTATION #DE487-58
FOR:BBN-ACI

THIS PRICING ASSUMES:

1. Processing: STANDARD COMMERCIAL (0 C to 70 C , VCC ±5%)

2. Minimum order guidelines: Sixty (60) day maximum between first and last requested delivery on purchase order.

- $7,500. COMMERCIAL

- If sufficient die in stock to cover assembly run, the minimum order would be:
  $5,500. COMMERCIAL

- $2,500. minimum on orders from box stock. Under $2.5k OK if order depletes existing stock.

IV. NON-RECURRING ENGINERRING SCHEDULE

Schedules provided are approximate and are to be used for planning purposes only.

STEP	TIME FROM PREVIOUS STEP
1NRE-ASS	*
2NRE-ASC	*
LAYOUT	1 WEEK/10K GATES
3NRE-APG	*
4NRE-ADP	6

* BOTH SIMCPL AND SIMAPG ARE CUSTOMER CONTROLLED.

V. PRODUCTION SCHEDULE

12 weeks ARO

VI. DESIGN INTERFACE

LEVEL	DESCRIPTION
IIA	All design work done at LSI Logic Design Center
IIB	Design work done at customer site using LDS III
IIC	Schematic capture done at customer site with SOFTWARE DATA BOOK
IID	Preliminary design work done at customer site with DESIGN VERIFIER
III	TURNKEY design with schematics, critical timing and test vectors from customer

LSI LOGIC CORPORATION
AND
HAMILTON/AVNET
SOFTWARE QUOTATION
FOR
BBN - ADVANCED COMPUTER, INC.

PROGRAM LICENSE PROPOSAL

Date: May 20, 1987
Quote Number: NEWG87-033A

SOFTWARE FOR SUN MICROSYSTEMS WORKSTATION	LICENSE FEE	ANNUAL MAINTENANCE
LDS III		
LDS GRAPHICS MODULE (LSED)		
COMPACTED ARRAY LIBRARY (LCA10K)		
MAINTENANCE AND INSTALLATION		
Program license and fee for two nodes	$60,000	INC.

One year license to run LDS simulator software on SUN Microsystems workstations running the Unix 4.2bsd operating system.

→ REL 3.2 SUMMARY 3.0

This license gives the user the ability to graphically capture schematics, generate net lists, do functional simulation, timing simulation and test extraction. Specifically, this system consists of the following modules:

LDS Graphics (LSED)
Wave Form Analysis (LWAVE)
Netlist Capture
Compile (LCMP)
Link (LLINK)
Delay Generator (LDEL)
Single Chip Simulator (LSIM)
Test Vector Extraction (LTEST)
Verify (LVER)
LCA10000 Series Compacted Array
Functional and Performance Libraries

PROGRAM LICENSE PROPOSAL (CONT.)

Date: May 20, 1987
Quote Number: NEWG87-033A

Also included in the program license fee is installation and training for LDS III on a SUN workstation.

The maintenance plan requires that BBN-ADVANCED COMPUTER, INC., set up an internal support group to act as the point of contact for software updates and problems or questions.

LSI LOGIC will apply the above program license fee to a full license if the conversion is done any time during the term of Program License.

Hamilton Avnet ELECTRONICS
An AVNET COMPANY

10 D Centennial Drive ☐ Peabody, Massachusetts 01960 (617) 532-3701

October 3, 1987

BBN
50 Moulton Street
Cambridge, MA 02238

Attention: Vince Santarlasci

Subject: Gate Array Quotation

Dear Vince,

Please accept the following quotation for a 223CPGA option on the LSI Logic Gate array.

LSI LOGIC DEVICE	PKG. TYPE	YEAR	1K	5K	10K
LCA10051	223CPGA	1988	$202.79	$140.51	$129.84

If you have any questions, please call me.

Sincerely,

Mark A. Trulli
ASIC Specialist

cc: Ward Hariman, BBN-ACI
Phil Levin, BBN-ACI
Jim Pena, LSIL
Lynne Roberts, H/A
Rupert Stanley, H/A

LSI LOGIC

LSI Logic Corporation
1551 McCarthy Blvd
Milpitas CA 95035
408.433.8000

INVOICE NO. 060148
SALES ORDER NO. DE004216
DATE 12/31/87

FROM
LSI LOGIC
LSI Logic Corporation
48580 Kato Rd
Fremont CA 94539

SHIP TO

SOLD TO
970020
HAMILTON AVNET
ASIC OPERATIONS DIVISION
1175 BORDEAUX DRIVE
SUNNYVALE, CA
94089

SHIP TO
090 BBN COMPUTER CORPORATION HA1
33 MOULTON STREET
CAMBRIDGE, MA
02138

ORDER DATE	TERMS	F.O.B.	SHIP VIA	PURCHASE ORDER NUMBER
12/31/87	NET 30	SHIP POINT	FED EX P1	94-000562

ITEM	QUAN. ORDER	QUAN. SHIP	QUAN. B/O	DESCRIPTION
				MONOLITHIC MICROCIRCUITS
SCN#751905184				
001	1	1	0	MDE: SW-S06-CRIT SN1104 =2 TIMING ANALYZER FOR LCAP 01/01/88 ( )
002	1	1	0	MDE: SP-S06-SUPP MAINT. FOR LCAP 01/01/88 ( )

EXPORT OF THESE COMMODITIES/TECHNICAL DATA CONTRARY TO US LAW IS PROHIBITED

We certify that articles/services listed and shipped herewith under above purchase order have been inspected and are in full accordance with the requirements of said purchase order and drawings/specifications applicable to that order. We certify that inspection evidence, including test data, necessary to substantiate this certification is available from our files.

Where materials/services incorporated in any of the items have been procured by LSI Logic from vendors, we certify that test reports and/or suitable evidence of compliance with the requirements of the above mentioned purchase order have been obtained by LSI Logic and are available from our files.

Quality Assurance Representative

Quality Assurance Stamp

DATE SHIPPED	SHIPPED BY	NO. BOXES	WEIGHT	CARRIER	WEIGHBILL NO.	FREIGHT CHARGES
12/31	992	1	3	Fed-Ex P1	885903006	$14.25

INSTRUCTIONS

1. COMPLETE ALL APPLICABLE UNSHADED BOXES.
2. DO NOT WRITE IN SHADED BOXES.
3. REQUISITIONER – RETAIN LAST COPY.
4. FORWARD TO NEXT HIGHEST APPROVAL REQUIRED.

REQUISITION

153835

REQUISITION DATE	REQUISITIONER	CHECK ONE
9 (Day) 12 (Month) 87 (Year)	Philip Levin	☒ ORIGINAL REQUEST ☐ CHANGE TO P.O. NO. _____ ☐ BLANKET P.O. NO. _____

DEPT. NO.	JOB NO.	ACCOUNT NO.
0 1 0	1 3 1 8 3 0	

GOVERNMENT CONTRACT NO.	GOVT. PRIORITY	GOVERNMENT PROPERTY
		☐ CONTROLLABLE ☐ EXPENDABLE ☐ DELIVERABLE

PCO	ACO	DATE ORDER PLACED
☐ ADVANCE NOTIFICATION REQUIRED ☐ WRITTEN CONSENT REQUIRED	☐ ADVANCE NOTIFICATION REQUIRED ☐ WRITTEN CONSENT REQUIRED	Day Month Year

INTERNAL DESTINATION	SHIP TO	TAXABLE
11/425 (Location) P. Levin (Person)	☐ 87 FAWCETT STREET, CAMBRIDGE, MA 02238 ☐ OTHER:	☐ YES ☐ NO

F.O.B.	SHIP VIA	SHIPMENT TERMS	PAYMENT TERMS	SUPPLIER NO.
		☐ PREPAID ☐ COLLECT		

SUGGESTED SUPPLIER	SELECTED SUPPLIER
LSI Logic 1601 Trapelo Rd. Waltham, MA 02154 ATTN: Jim Pena	

ITEM	QUANTITY	U/M	DESCRIPTION	DELIVERY REQUIRED (Day Mo. Year)	ESTIMATED PRICE	UNIT PRICE	REMARKS
1	1		SW-509-CRIT Timing Analyzer (LCAP)		~~$15,000.~~		
2	1		MT-509-CRIT Maintenance for LCAP		no charge		
			BBN agrees that the LCAP module will be governed by the terms and conditions of the software license agreement between LSI Logic and Bolt, Beranek & Newman, Inc. dated June 25, 1987. This license remains in full force and effect.				
					$12,000		
UNIT OF MEASURE CODE: BX-Box, C-Hundred, CS-Case, CT-Carton, CY-Cylinder, DA-Day, DR-Drum, DZ-Dozen, EA-Each, FT-Foot, G-Gram, GL-Gallon, GR-Gross, KG-Kilogram, L-Litre, LB-Pound, LT-Lot, M-Thousand, ME-Meter, MO-Month, OZ-Ounce, PR-Pair, PT-Pint, QT-Quart, RL-Roll, ST-Set, TO-Troy Ounce, YD-Yard				EST. TOTAL ▶	~~$15,000.~~	TOTAL ▶	

REMARKS (Requisitioner to Buyer)	APPROVAL SIGNATURES		REMARKS (Buyer to Supplier)
	REQUISITIONER DATE	NAME DATE	
	NAME DATE	NAME DATE	
	NAME DATE	NAME DATE	
	NAME DATE	NAME DATE	

REQUISITIONER

LSI LOGIC

December 23, 1987

Mr. Philip Levin
BBN Communications Corporation
50 Moulton Street
Cambridge, MA 02238

Dear Phil:

LSI Logic and Hamilton/Avnet are pleased to present this quotation for our Path Timing Analyzer Tool (LCAP). This quotation has been assigned number NEWG87-085A for future reference.

LCAP enables the user to identify and receive reports on the timing of critical paths in his design independent of all simulation vectors (examine the timing of all paths, including paths emanating from a single point). LCAP also allows the user to define the paths to be examined.

At each step in the design cycle, inconsistencies may arise between a proposed solution and the original design goals. These inconsistencies can require the designer to iterate the design cycle, increasing the time and cost. The Timing Analysis Tool speeds up the design cycle by providing a fast way to analyze timing of specific paths in a circuit.

LCAP is a static analysis tool. A static analysis tool has three notable advantages: 1) it is fast, 2) it can accommodate large designs (over 200,000 transistors/50,000 gates), and 3) its results are independent of input patterns. LCAP satisfies this need for speed by using simplified, local analysis of delay values of network components. The operating condition is defined by the user.

As we discussed, we have quoted this additional module for your existing Sun-based design system.

The ordering information for LCAP is:

Part #	Description	Price
SW-SO6-CRIT	Timing Analyzer (LCAP)	$12,000
MT-SO6-CRIT	Maintenance for LCAP	Included

The price for additional copies is $3,000 per copy.

This pricing is for additions to the existing license. Therefore, this module license will have the same termination date as the other software.

BBN can add this module to the existing license by including on your purchase order the following phrase:

> "BBN agrees that the LCAP module will be governed by the terms and conditions of the software license agreement between LSI Logic and Bolt Beranek & Newman, Inc. dated June 25, 1987. This license remains in full force and effect."

If you have any questions, please feel free to contact me.

Sincerely yours,

LSI LOGIC CORPORATION

William N. Giudice

William N. Giudice
Area Software Sales Manager

WNG/dac
cc: Jim Pena, LSIL, MA
Arthur Babitz, BBN
Lynn Roberts, Hamilton/Avnet

LSI LOGIC

October 16, 1987

EO

Mr. Philip Levin
BBN Communications Corporation
50 Moulton Street
Cambridge, MA 02238

Dear Phil:

LSI Logic and Hamilton/Avnet are pleased to present this quotation for our Path Timing Analyzer Tool (LCAP). This quotation has been assigned number NEWG87-085 for future reference.

LCAP enables the user to identify and receive reports on the timing of critical paths in his design independent of all simulation vectors (examine the timing of all paths, including paths emanating from a single point). LCAP also allows the user to define the paths to be examined.

At each step in the design cycle, inconsistencies may arise between a proposed solution and the original design goals. These inconsistencies can require the designer to iterate the design cycle, increasing the time and cost. The Timing Analysis Tool speeds up the design cycle by providing a fast way to analyze timing of specific paths in a circuit.

LCAP is a static analysis tool. A static analysis tool has three notable advantages: 1) it is fast, 2) it can accommodate large designs (over 200,000 transistors/50,000 gates), and 3) its results are independent of input patterns. LCAP satisfies this need for speed by using simplified, local analysis of delay values of network components. The operating condition is defined by the user.

As we discussed, we have quoted this additional module for your existing Sun-based design system.

The ordering information for LCAP is:

Part #	Description	Price
SW-SO9-CRIT	Timing Analyzer (LCAP)	$15,000
MT-SO9-CRIT	Maintenance for LCAP	Included

The price for additional copies is $3,000 per copy.

This pricing is for additions to the existing license. Therefore, this module license will have the same termination date as the other software.

BBN can add this module to the existing license by including on your purchase order the following phrase:

> "BBN agrees that the LCAP module will be governed by the terms and conditions of the software license agreement between LSI Logic and Bolt Beranek & Newman, Inc. dated June 25, 1987. This license remains in full force and effect."

If you have any questions, please feel free to contact me.

Sincerely yours,

LSI LOGIC CORPORATION

Bill Giudice

William N. Giudice
Area Software Sales Manager

WNG/dac
cc: Jim Pena, LSIL, MA
Arthur Babitz, BBN
Lynn Roberts, Hamilton/Avnet

10 Fawcett Street, Cambridge, MA 02238
Telephone 617-873-6000

November 28, 1988

BBN Advanced Computers Inc.

Rupert Stanley
Hamilton Avnet
10 D Centennial Drive
Peabody, Massachusetts 01960

Dear Rupert,

This letter is confirmation of the fact that BBN ACI wishes to purchase 7 pieces of the L1A3496 remaining from the initial prototype flow. These pieces will be applied to the existing BBN P.O. # 77190 at the stated price of $293.54 each.

Thank You,

Philip Levin
BBN ACI

Philip Levin
BBN Advanced Computers Inc.
10 Fawcett Street
Cambridge, Ma. 02148
(617) 873-2902

May 4, 1988

INTRODUCTION

This document is intended as a guide for the ~~trial~~ FINAL layout of the L1A3496 in the an LCA10051 die. It discusses the special clocking scheme of the L1A3496 and identifies and describes the critical nets.

THE BASIC DESIGN

Figure 1 shows the basic block diagram of the design. Note that the four major blocks operate on separate clocks. These clocks are completely independent and are derived from separate pins. Synchronization between the blocks has been accounted for.

The latch shown Figure 1 represents approximately 110 latches that are used to increase hold time on the TBUS module (QH and QT have a defined phase relationship).

In the general, the design has the following characteristics:

- just under 20,000 gates
- all random logic, no meagfunctions
- approximately 3.4 pins/net
- highly bus structured
- I/O intensive - all pins are used

IMPROVEMENTS FOR SPEED

Unfortunately, if the clock nets shown in Figure 1 were specified as clock nets and driven directly with a clock drivers, loading on those nets would force the "clock-to-Q" delay of the four modules to be unacceptably large. To get around this problem, I implemented the scheme shown in Figure 2.

Here, an external clock directly drives a set of "front-end" flip-flops to achieve the desired clock-to-Q delay. The "second-level" clock for each module is derived from that first level of drivers. Note that the CIO module does not have the clock-to-Q problem.

To reduce the number of specially handled clock nets, I have only specified the "second-level" nodes as clock nets (heavy lines). Therefore, the "first-level" nets will NOT have a guaranteed <2ns skew between elements on this net. This should not pose a problem since first-level clocked elements do not "talk" to each other - they only receive data from the second-level clocked elements.

In addition, there should be no hold-time violation between the second-level and the first-level clocked elements because the second-level clock always lags the first-level clock (the DRV8I's are heavily loaded). Therefore, I don't expect the timing alone will cause any problems, my concern is the layout.

PROPOSED LAYOUT

I have already used LPACE to group the top-level hierarchies (there are 18 of them) into three sections. This grouping should facilitate layout of the multi-clock scheme. Figure 3 shows some aspects of a proposed layout.

Note that the left half of the chip is devoted to the ~~UT_CLK/Z~~ U_TI_DA/BUF_TCLK clock net. I felt the best way to handle the other two clock nets, U_RQ_IO/BUF_TX_CLK and U_SV_IO/SRVR_CLK, was to divide the chip into top and bottom halves as shown. In the .CFUN file, I have specified the three sections as "reigons" to prevent swapping cells out of their "clock-zone."

CRITICAL NETS

The following are the critical nets:

NET: UT_ENA_HOLD/Z
COMMENT: THIS NET IS VERY IMPORTANT!! It has a fanout of 110. I do NOT care about skew between elements on this net but I DO care about the worst-case delay from the pin. This delay must be less than 5 ns.

Please treat this net as a "pseudo" clock net. That is, make it as wide as reasonably possible without making it a clock trunk driven from the top/bottom of the chip. Again, I don't care about sticking to the 2 ns max skew BETWEEN elements, I am just interesed in the maximum skew of the "last" element. I also believe that the buffer is unreasonably large and would like to be able to use a DRVT8.

NET: UT_CLK/Z
COMMENT: This nets' connection to the clock trunk buffer drivers, U_TI_DA/U_DRV8IA(A) and U_TI_DA/U_DRV8IB(A) as short as possible.

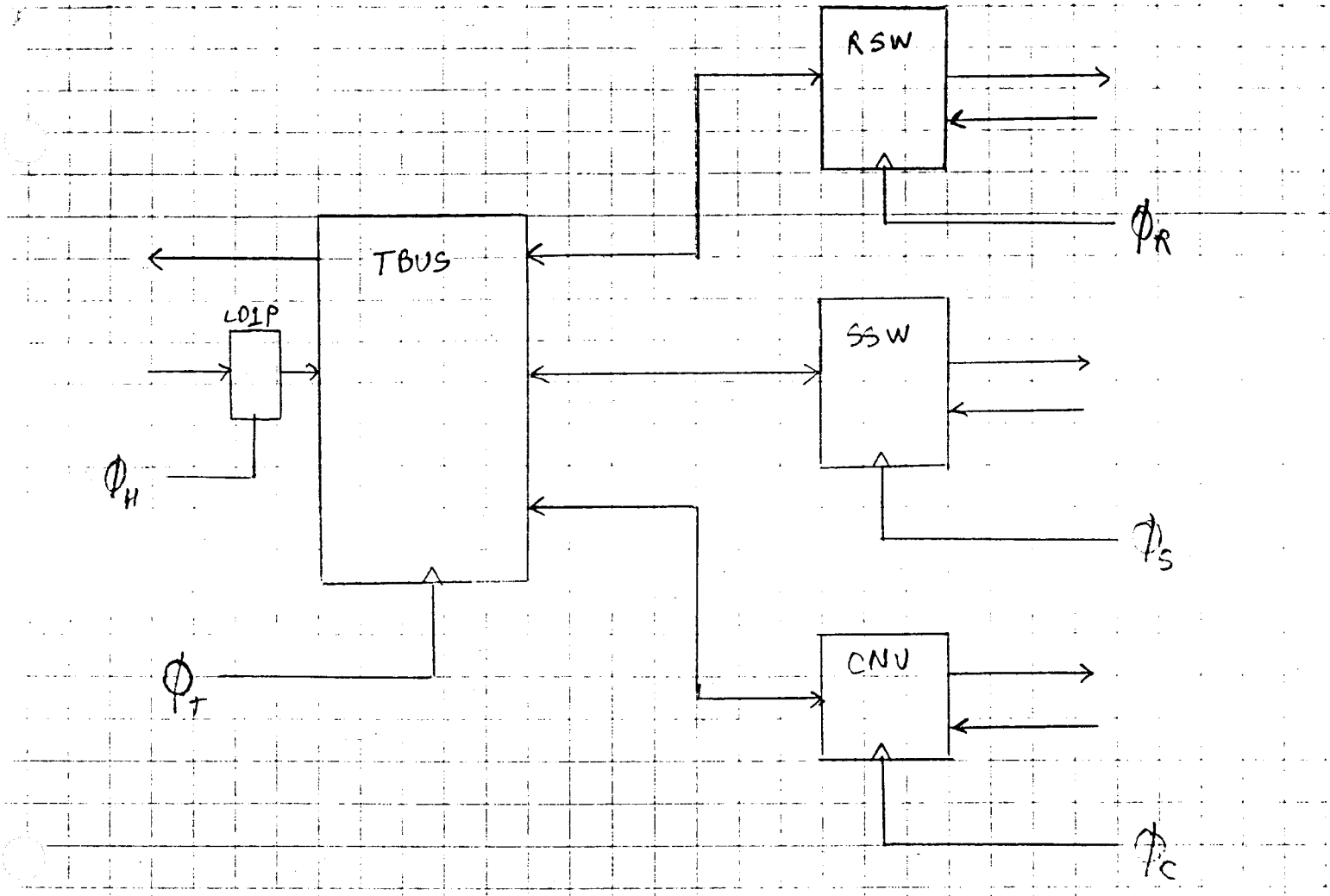
In addition this nets' connection to the 117 flip-flops of output stage should be as short as possible.

NET: UR_CLK/Z
COMMENT: This nets' connection to the clock trunk buffer drivers, U_RQ_IO/U_DRV8IA(A) and U_RQ_IO/U_DRV8IB(A) as short as possible.

NET: US_CLK/Z
COMMENT: This nets' connection to the clock trunk buffer drivers, U_SV_IO/U_DRV8I(A)

NETS: U_TI_DA/ENA_TDAT_OUT.2 through U_TI_DA/ENA_TDAT_OUT.0
U_TI_DA/ENA_TRANS_OUT.1 through U_TI_DA/ENA_TRANS_OUT.0
UF_CLK,
UR_REVERSE/Z,
US_FRAME/Z,
UR_DATA.7 through UR_DATA.0,
US_DATA.7 through US_DATA.0,
COMMENT: Please make as short as possible

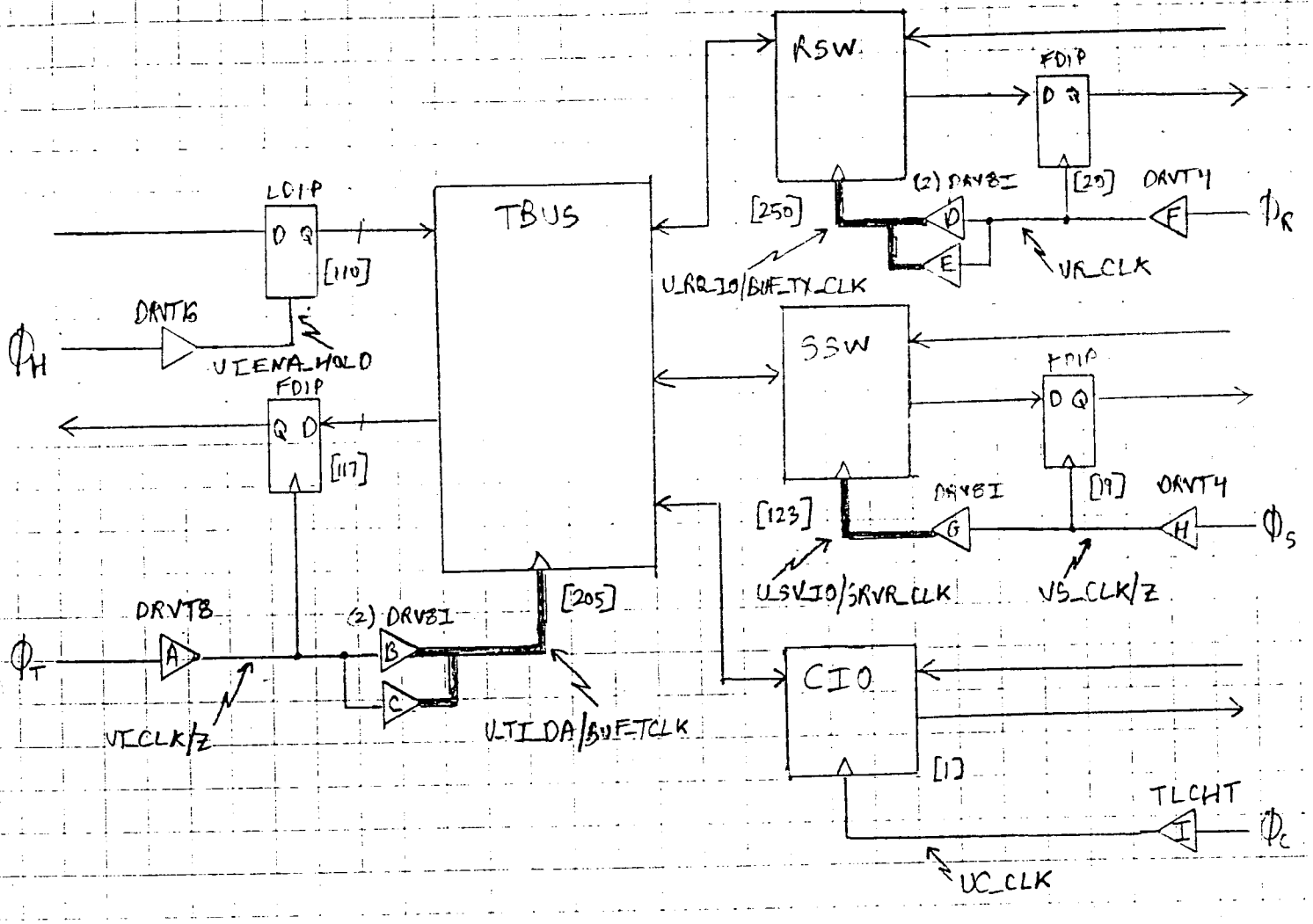
Thank You,
Phil Levin



BLOCK DIAGRAM – CLOCKING SCHEME

FIGURE 1

1/8/87 CPL

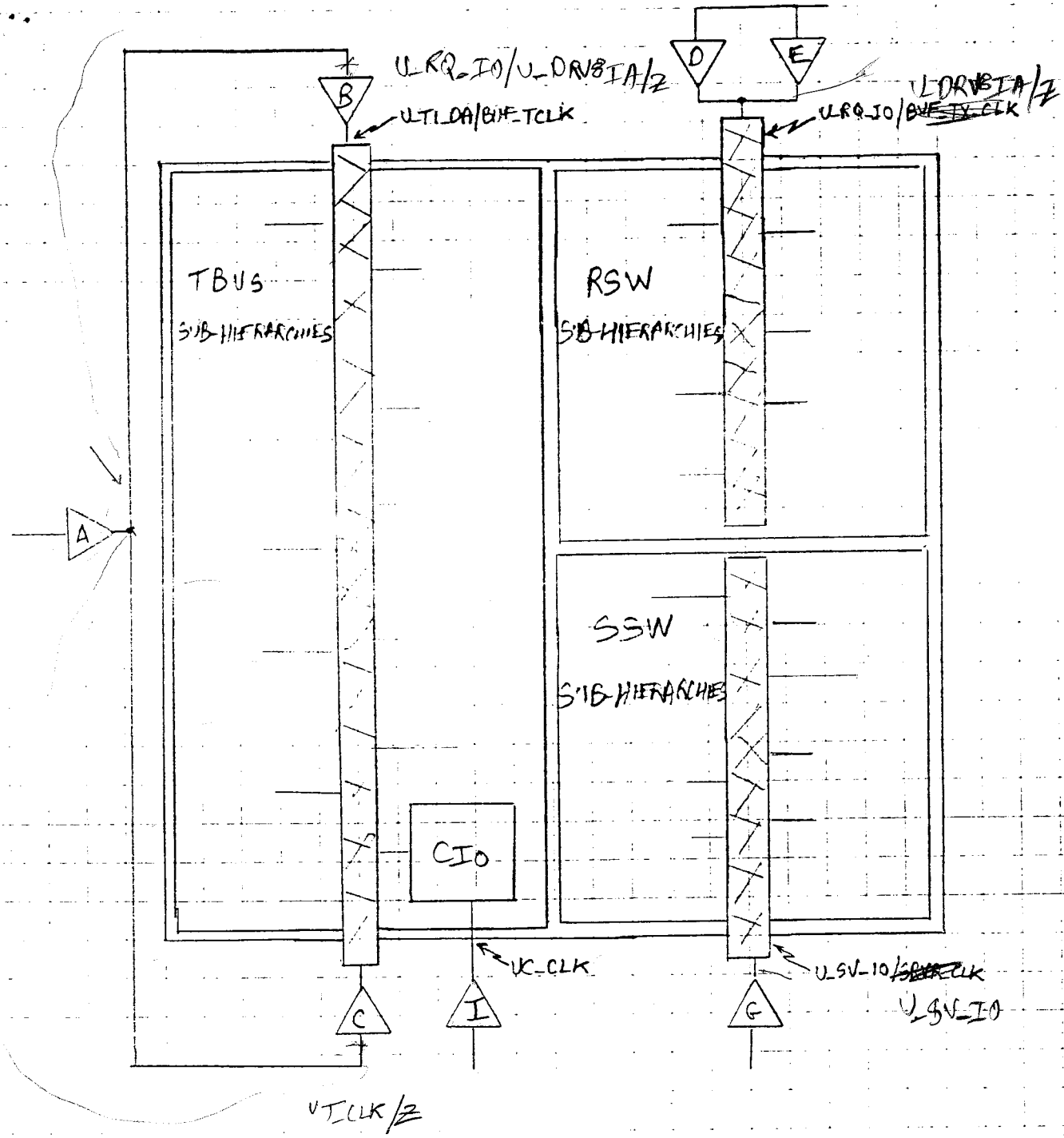


SPECIALLY TREATED CLOCK NETS (INDICATED WITH HEAVY LINES)

SCHEMATIC - CLOCKING SCHEME

FIGURE 2

1/8/85CPL



LAYOUT DIAGRAM - CLOCKING SCHEME

FIGURE 3

1/14/88 SPL

Philip Levin
BBN Advanced Computers Inc.
10 Fawcett Street
Cambridge, Ma. 02148
(617) 873-2902

June 20, 1988

Mano Vafia
LSI LOGIC 1501 McCarthy Boulevard
Milpitas, California 95035
FAX #: (408) 433-7720

cc: Suzzane Deeth, LSI California
Mark Halberstein, LSI Waltham
Jim Pena, LSI Waltham

Dear Mano:

I have reviewed the tape of the latest clocking structure for the L1A3496. The preliminary results show that there is a potential hold-time problem relating to the T_CLK/Z net. Please review the attached document regarding this problem and contact me to discuss your thoughts on it.

I will be working late every night this week, so please feel free to contact me during your own business hours.

Thank you for your help and cooperation. I look forward to hearing from you.

Sincerely,

Philip Levin

Philip Levin
BBN Advanced Computers Inc.
10 Fawcett Street
Cambridge, Ma. 02148
(617) 873-2902

June 20, 1988

INTRODUCTION

This document desribes a potential hold-time problem on the L1A3496 relating to the net: UT_CLK/Z. It also suggests a possible solution that involves only layout changes and not network changes. It may be useful to refer to the initial L1A3496 layout document, dated May 4, 1988 while reading this document.

STRUCTURE OF THE PROBLEM AREA

Figure #1 shows the schematic of the relavant portion to the circuit. Note that there are about 117 "output registers" and about 208 "core registers".

The problem is that the last "output register" F/F to be clocked on the net, UT_CLK/Z, must be clocked BEFORE the first "core register" F/F attached to the net, U_TI_DA/BUF_TCLK. Of course, this is a very conservative approach because as shown, there is at least one level of combinatorial logic between the core registers and the output register. In addition, the core registers will always have some minimum clock-to-q delay.

Figure #2 shows the current layout structure of the elements in Figure #1. The "special" branches A and B (of the UT_CLK/Z net) are used to provide a balanced path from the predriver (UT_CLK) to the postdrivers (U_TI_DA/U_DRV8IA, U_TI_DA/U_DRV8IB).

THE PROBLEM

Unfortunately, those special branches are a little TOO FAST relative to the rest of the branches of UT_CLK/Z to the output registers. This causes the earliest clocking F/F in the core logic to receive its clock very close to the latest clocking F/F in the output register. Some numbers from LDEL using the SEGLEN file are below:

At WCCOM:

Earliest clocking "core" F/F delay from CLK PIN =	6.86 ns
Latest clocking "output" F/F delay from CLK PIN =	5.47 ns

	1.39 ns

At BCCOM:

Earliest clocking "core" F/F delay from CLK PIN =	2.35 ns
Latest clocking "output" F/F delay from CLK PIN =	2.45 ns

	-0.10 ns

So, at BCCOM there is negative margin. In reality this margin does not cause any problem because the minimum clock-to-q delay of a F/F in addition to the minimum delay caused by the data path will probably dominate this small amount of skew. And, of course, this amount of negative skew probably occurs safely in other places.

My concern is that in this case, the wire delays are dominating the transistor delays. Any variation in the wire delay model will have a greater effect in a possible hold-time violation. In other words, the simulator may not complain (so far it has not), but the silicon may not work.

IS THIS REALLY A PROBLEM?

Should I be concerned? Is this enough margin? If not, I have a solution to increase the margin.

PROPOSED SOLUTION

Refering to Figure #3, I think the problem should be attacked from two angles: 1) speed-up the UT_CLK/Z net, and 2) skew the U_TI_DA/U_DRV8IA net even more, relative to the UT_CLK/Z net. This is accomplished as follows:

Speed-up the UT_CLK net: Add a "pseudo" clock net trunk from which tributaries to the output logic are attached. This should be done exactly as it was done for the T_ENA_HOLD net (not shown), making a trunk of the same width.

Skew the U_TI_DA/U_DRV8IA clock net: Leave the two special branches (A and B) basically intact but add some balanced serial delay (about 1.2 ns @WCCOM) by increasing their length or adding loads (whatever you think is the best way).

CONCLUSION

Please let me know what you think.

Thank You,

Phil Levin

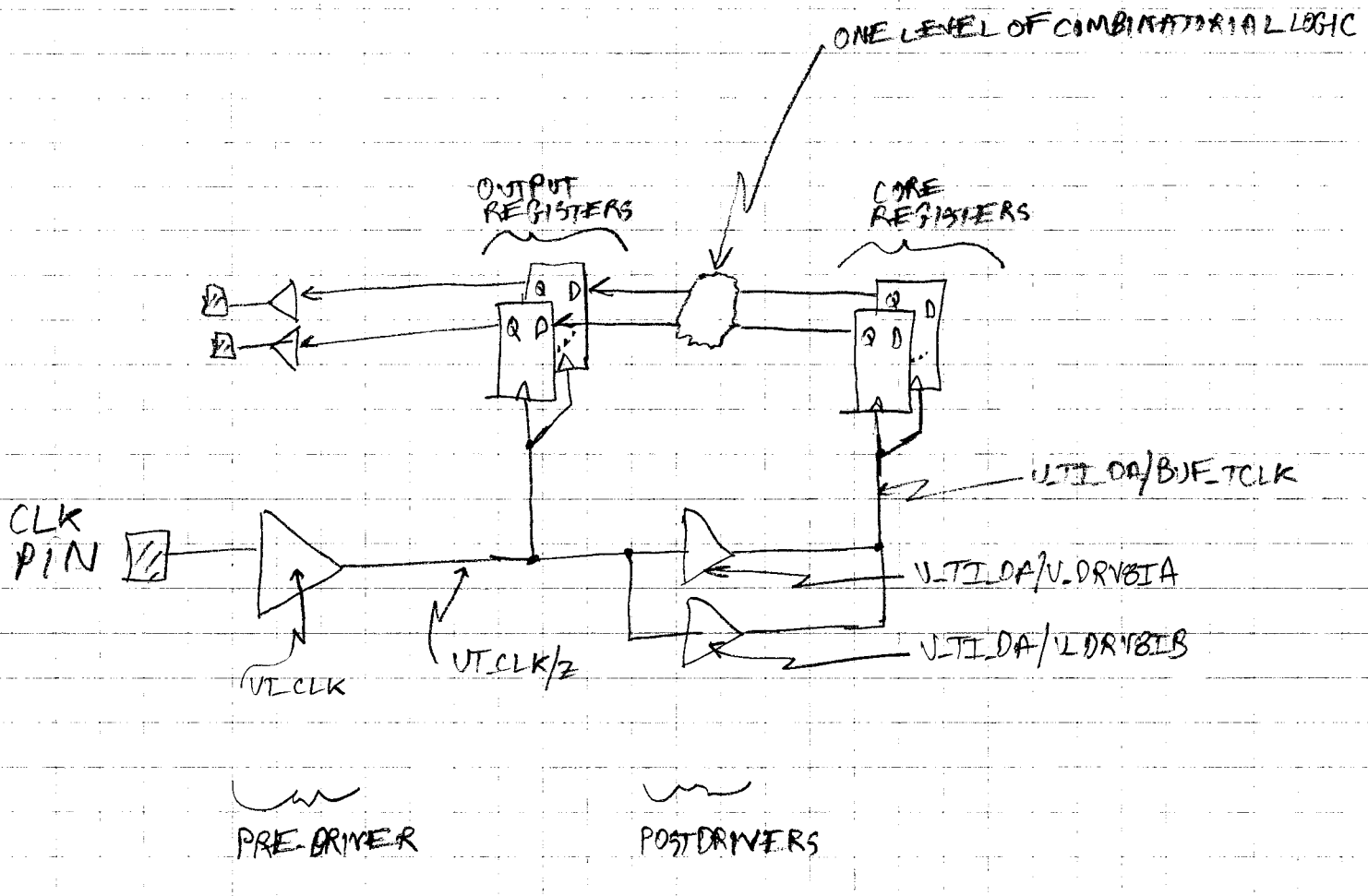
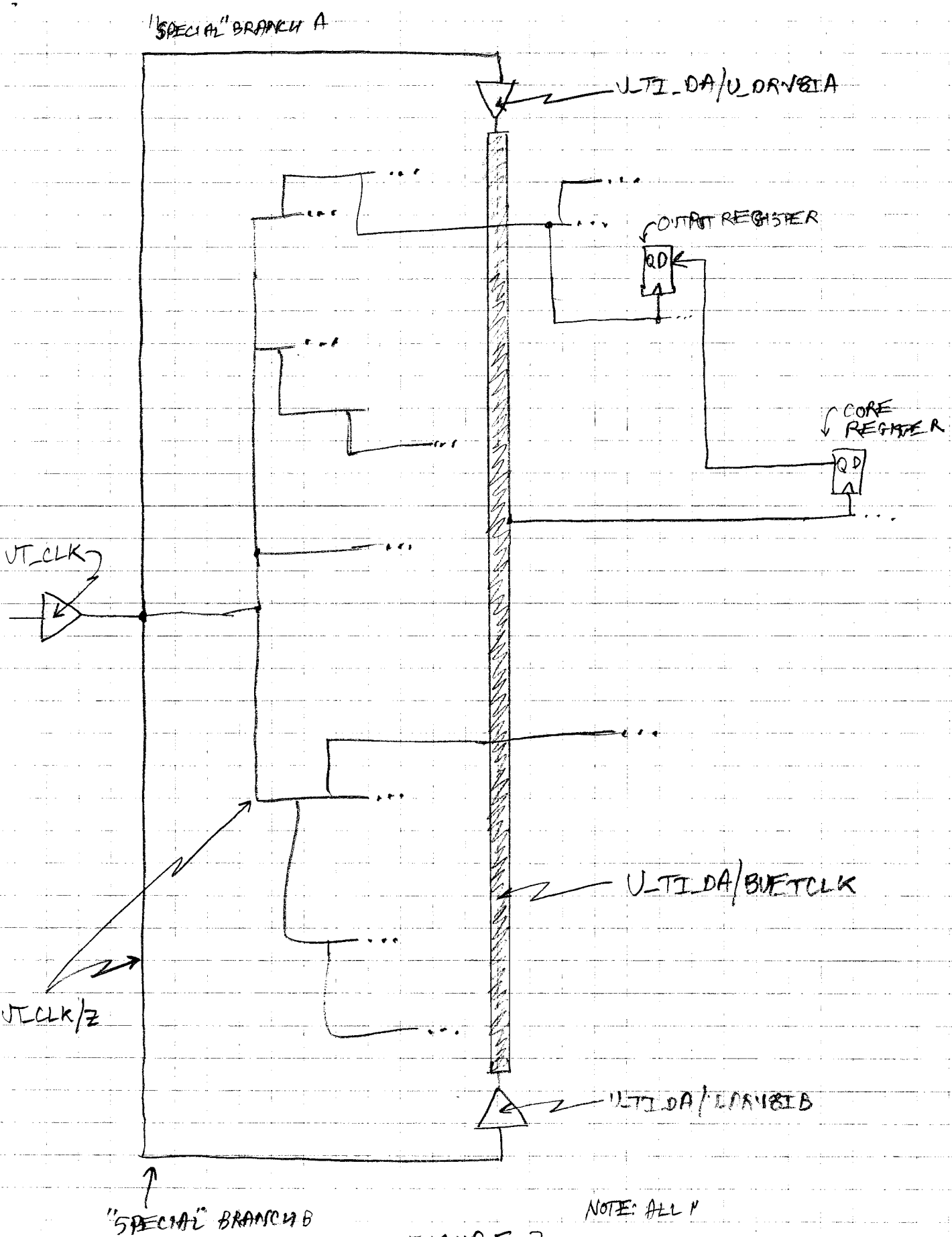


FIGURE 1

CURRENT CLOCKING SCHEMATICS

6/20/88 CPL



NOTE: ALL I

FIGURE 2

CURRENT CLOCKING SCHEME

6/20/88 CPL

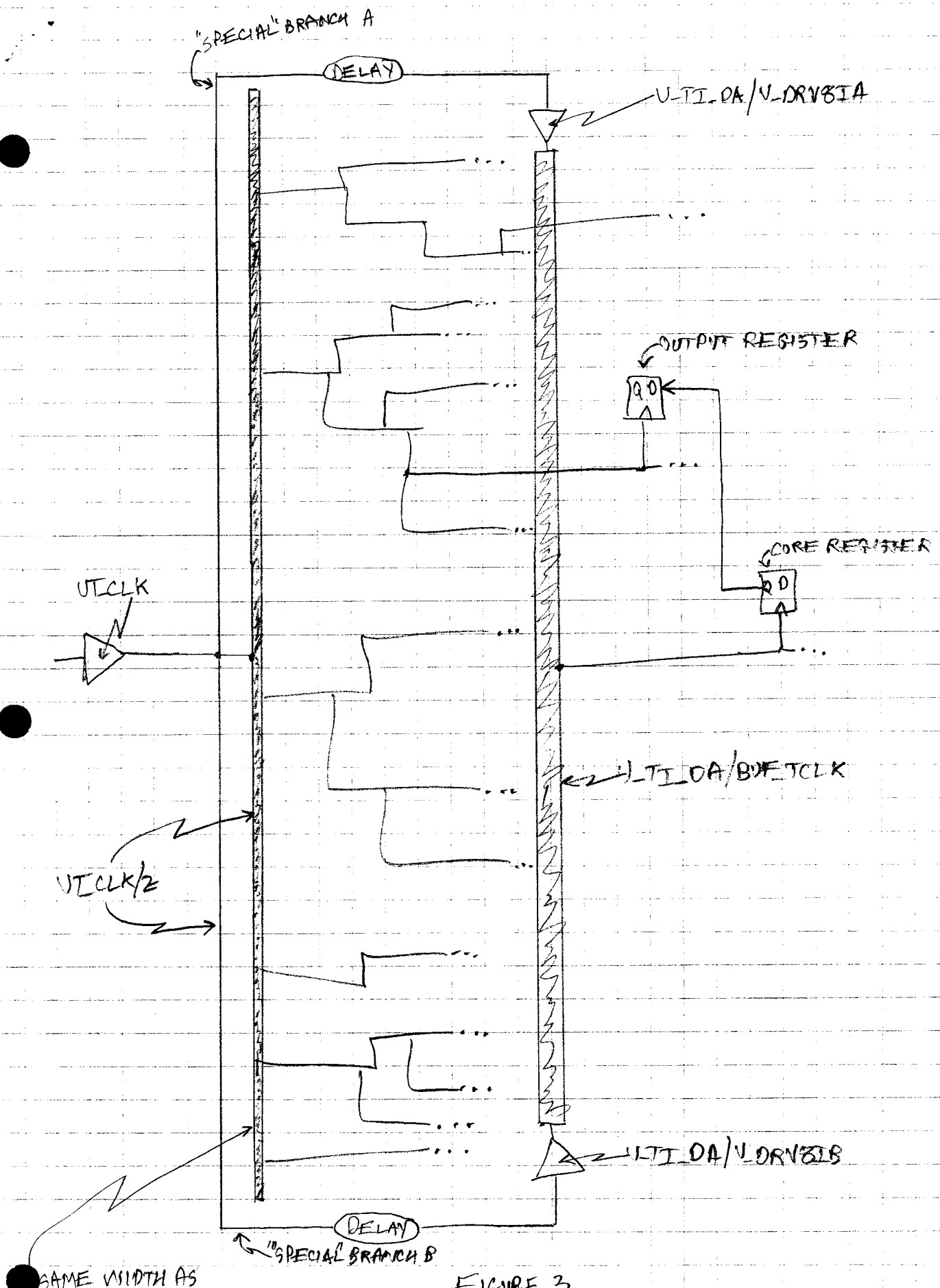


FIGURE 3

NEW CLOCKING SCHEME

6/20/88 CPL

Philip Levin
BBN Advanced Computers Inc.
10 Fawcett Street
Cambridge, Ma. 02148

January 18, 1988

INTRODUCTION

I am currently designing a gate array with LSI using the LCA10075 compacted array. After conversations with my local Applications Engineer, I became concerned that my rather unusual clocking scheme may be difficult to handle in layout. This design presentation is aimed at informing the people most closely associated with the actual layout of my intentions. From this, I hope to anticipate any problems that I may encounter, so that I can make any necessary changes well before layout.

THE BASIC DESIGN

Figure 1 shows the basic block diagram of the design. Note that the four major blocks operate on separate clocks. These clocks are completely independent and are derived from separate pins. Synchronization between the blocks has been accounted for.

The latch shown Figure 1 represents approximately 50 latches that are used to increase hold time on the TBUS module (QH and QT have a defined phase relationship).

In the general, the design has the following characteristics:

- approximately 20,000 gates
- all random logic, no meagfunctions
- approximately 3.6 pins/net
- highly bus structured
- I/O intensive - all pins are used

IMPROVEMENTS FOR SPEED

Unfortunately, if the clock nets shown in Figure 1 were specified as clock nets and driven directly with a clock drivers, loading on those nets would force the "clock-to-Q" delay of the four modules to be unacceptably large. To get around this problem, I implemented the scheme shown in Figure 2.

Here, an external clock directly drives a set of "front-end" flip-flops to achieve the desired clock-to-Q delay. The "second-level" clock for each module is derived from that first level of drivers. Note that the CIO module does not have the clock-to-Q problem.

To reduce the number of specially handled clock nets, I have only specified the "second-level" nodes as clock nets (heavy lines). This should not pose a problem since first-level clocked elements do not "talk" to each other. In addition there should be no hold-time violation between second-level and first-level clocked elements because the second-level clock always lags the first-level clock (the DRV8I's are heavily loaded).

Therefore, I don't expect the timing alone will cause any problems, my concern is of course: layout.

PROPOSED LAYOUT

I have already used LPACE to group the top-level hierarchies (there are 18 of them) into three sections. This grouping should facilitate layout of the multi-clock scheme. Figure 3 shows some aspects of a proposed layout.

Note that the left half of the chip is devoted to the Tb clock net. I felt the best way to handle the other two clock nets, Rb and Sb, was to divide the chip into top and bottom halves as shown. I will ensure that the buffers will have the correct placement. In the .CFUN file, I will specify the three sections as "reigons" to prevent swapping cells out of their "clock-zone."

QUESTIONS

Besides the general question: "what do you think?" I have the following, more specific questions:

1) Will the "reigons" specification from LPACE be enough to prevent swapping out of the sections?

2) What will the max clock skew be between any two clocked elements in any of the three reigons?

3) Are there any recommendations for improvements?

Phelps Tom

LSI LOGIC

MEMO

TO: JIM PENA

FROM/EXT: BILL GIUDICE Bill

SUBJECT: BBN SOFTWARE PROBLEMS

DATE: FEBRUARY 29, 1988

This memo is to update you on the latest status of BBN's software problems and enhancement requests. The list below reflects those items covered in my memo dated January 18, 1988. Please forward the following response to BBN and thank them for their good inputs.

LSED Issues:

1) Hardcopy - there appears to be no way to get reliable hardcopy of anything but tiny drawings that clearly fit on a page. The infinite sheet theory works only with infinite printers.

1a) Does Postscript hardcopy on 11 x 17 paper work?

Currently the only Postscript filter that is available and supported, is for A size paper. We are currently looking into numerous plotting enhancements that will eventually correct some of these limitations, but no schedules have been released.

2) Lack of DEMORGAN equivalents and logical assertion checking.

This feature is currently under evaluation. If it proves feasible, it will be incorporated into a future release.

3) The "undo" command does not work.

We are aware that this command is cumbersome to use and are currently investigating alternatives to solving this issue.

4) There seems to be a bug with grounded wires going into bus extractors.

Zdzislaw is in the process of analyzing the test case which exhibits this problem. We will keep you updated on its status.

5) Phil has suffered about a dozen unexplained and not repeatable crashes in the past six months (using version 7).

Version 7.0 had a problem with the DEF files which occasionally caused LSED to crash. Version 8.0 has corrected the DEF problem but older 7.0 designs may still cause LSED to crash. Please install version 8.0 and let us know if you experience further problems.

6) LSED requires an entire design to be in core at once to edit any of it. While this results in good response for small designs, it produces enormous core images for even a few thousand gates.

LSED was designed to load the entire design database into memory so that the designer can traverse up and down the hierarchy at any time without having to save and reload an upper level. Additional main memory will help alleviate this problem.

If you plan to work on only one level of the hierarchy, then just that level can be loaded into LSED, i.e., use:G to get just the desired level and all of its circuitry below.

7) Reading and writing files is too slow. Checkpointing is too slow.

There is no current fix to this problem, but we are looking into ways of speeding up the processes. Again, additional main memory will help alleviate this problem.

8) The automatic router results in difficult-to-read schematics. In addition, it may place wires on top of each other, or on top of bodies.

The router uses the Lee algorithm. The only time a wire is placed on top of another wire, or body, is when there is no area to route over. In other words, routing is limited by the wires and bodies around it. This can happen when a group select has been used, followed by a group move. In release 9, all elements in a group will remain unaltered. This should make the schematics more readable.

In addition, version 9.0 will contain an auto router disable switch and possible some wire editing features.

9) There is no way to rotate or mirror bodies.

This enhancement has been included in release 9.0.

10) Moving connectors on symbols doesn't seem to work.

Release 9 will also contain a fix for this problem.

11) There's no way to see what text is attached to.

This is an excellent suggestion. An enhancement in release 9 will allow the designer to toggle (A key) the text and highlighted attachment point.

12) Text can't be sized.

Currently, there is a :SIZE command, but without the above enhancement, text might be reduced in size to make in unreadable and undetectable. This command will be documented in release 9.0.

13) Labels on symbols and nets that fall partly outside the window are not drawn at all.

This problem has been fixed in release 9.0.

14) The mechanism to prevent a quit without saving changes does not work before the first save.

We have been unable to reproduce this failure here. Please send us more information on the exact sequence of commands needed to reproduce this problem.

15) LSED and associated tools use a flat directory structure. A large design has so many files that the directory become unmanageable.

These tools were designed to be used in the same working directory. This may be changed in a future release.

16) There is only one 'group' possible at one time, and it evaporates after use.

The disappearing of the group select, after the use, is changed in release 9.0. It must be deselected by using the space bar, just like selecting a symbol.

If selecting multiple groups simultaneously is also needed, we would like to further discuss this possible enhancement with you.

17) The 'delete' and 'move' keys are too close together!

Separating these keys was tried and found to be unsuccessful during a beta test of a recent release.

18) There is a 512 character limit on the TYPE list. This can quickly cause problems on large busses with long signal names. There is no line continuation character for the "lsedinit.do" file.

Both of these problems will be fixed in release 9.0.

LCMP, LLINK Issues:

1) Modules must be compiled in the right order to avoid warning messages.

Warning messages within LCMP and LLINK are important in flagging possible design problems. We will consider the possibility of offering a disabling option for some of the warnings.

2) Warnings about unconnected outputs can't be controlled or suppressed.

Same as item #1.

3) There's an unexpected 8 character restriction on module name length.

Top level modules are limited to 8 character names. Lower level modules may accommodate more characters, but we recommend that the name not exceed 8 characters. This limitation is IBM platform related and cannot be changed.

4) Binary files produced by the compiler, linker, and simulator are unobservable preventing us from tracking down problems or writing our won analysis software.

There are many reasons for keeping certain design files in binary form. One reason is that editing these files could seriously corrupt the design data causing major problems for both the user and LSI Logic. There are no current plans to change binary files to ASCII format.

5) Are version 8.0 net files encrypted or not? The change not says yes, but he software doesn't seem to behave that way.

Version 8.0 net files are not encrypted. The documentation reflected the original plans which were not implemented.

6) LVER and LDEL documentation is out of date. It is very difficult to follow the file name, and procedure changes using the release notes.

Technical Update Bulletins (TUBs) are issued with every software release and are appended to the manuals. The manuals are periodically revised to include all of the TUB information.

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This problem has been corrected in release 9.0.

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LCAP is a new product and has unfortunately suffered from limited documentation. We are currently in the process of updating the manual and hope it will be much easier to follow.

3) Cannot use batch-mode for turning on and off paths. This makes regression testing EXTREMELY difficult.

We are currently evaluation this feature as a future enhancement. No schedule set.

4) Cannot specify that a transparent latch is enabled. LCAP uses the D-input / Q-output as a Start/Stop instead of modelling a latch as a pass-through delay element.

We would like to obtain more information regarding this problem and will be contacting you shortly.

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We will be making the appropriate changes to LSED as that this crash does no occur in the future releases.

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This crash may be related to improper use of the BID modifier on busses. For example, incorrect: B(#IN);OUT;TYPE=(4)
correct: B$(#IN);OUT;TYPE=[4]
See 7.1 TUB for further details. Release 8.1 will not allow LWAVE to crash with this error.

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We have not experienced any problems with LCAP rlogins. This problem may be system related and we'll need to get more details on your exact configurations.

4) LSIM - when used with release 7 net list / SIM file.

Release 8.0 requires that all modules be recomplied. 7.0 net files are compatible with 8.0 and will not cause any problems. We will look into trapping this error so that LSIM does not crash with future releases.

BG:sacs

To: Bill Giudice
From: Zdzislaw Marcisz
Subject: BBN Software Problems

February 10, 1988
cc: List

This memo is to update you on the latest status of BBN's software problems and enhancement requests. The list below reflects those items covered in your memo dated January 18, 1988. Please forward the following response to BBN and thank them for their good inputs.

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List:

Jim Pena
Jim Smith
Brian Connors
Paul Bergantino
Bob Blair
Issy Curtin
Van Lewing
Tom Daspit
Fred White
Rangu Ranganathan
Dan McMullen
Sondra Wroblewski
Greg Damon
Jim Koford
Tom Willwerth
John Swenson

LSI LOGIC

March 3, 1988

Mr. Philip Levin
BBN Advanced Computers, Inc.
10 Fawcett Street
Cambridge, MA 02148

Dear Phil,

Thank you for taking the time to document your questions, concerns, and problems with LSI Logic's ASIC Design Software.

The attached memo was compiled and reviewed by our technical software and CAD group and should address each of the items you described.

LSI Logic feels the LDS software package running on the Sun Microsystems Platform is one of the best ASIC development systems available. But, we also depend on customer feedback to make needed refinements and enhancements.

We appreciate your openness, and hope that you will continue to let us know of any areas where improvements can be made. If you have any questions regarding the attached, please let Bill Giudice or myself know.

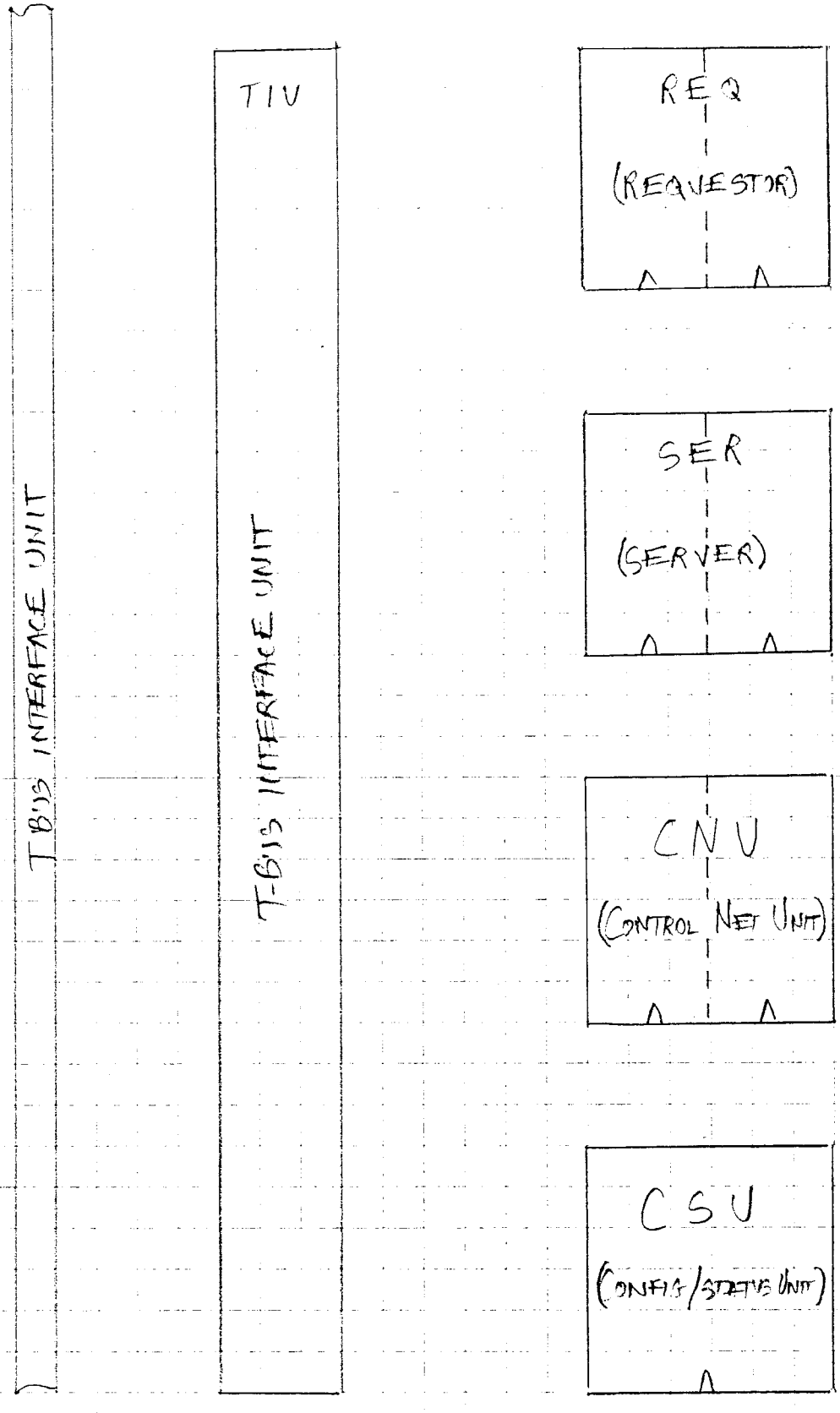
Sincerely,
LSI LOGIC CORPORATION

Jim Pena
Field Sales Engineer

JP:sacs

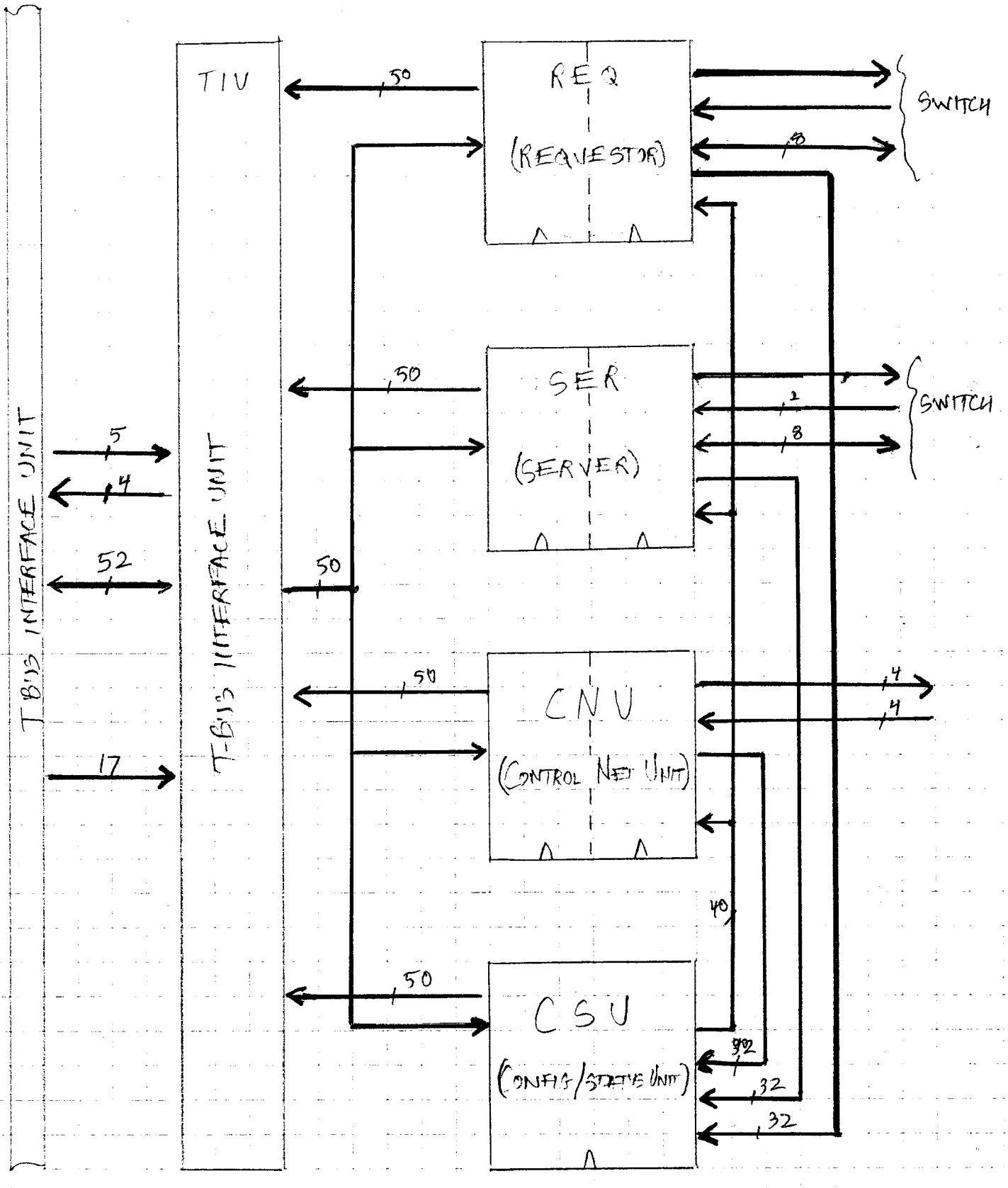
Attachment:

CC: Guy Ferdorkow
John Goodhue
Dan Fradkin
Bill Giudice



SIGA BLOCK DIAGRAM

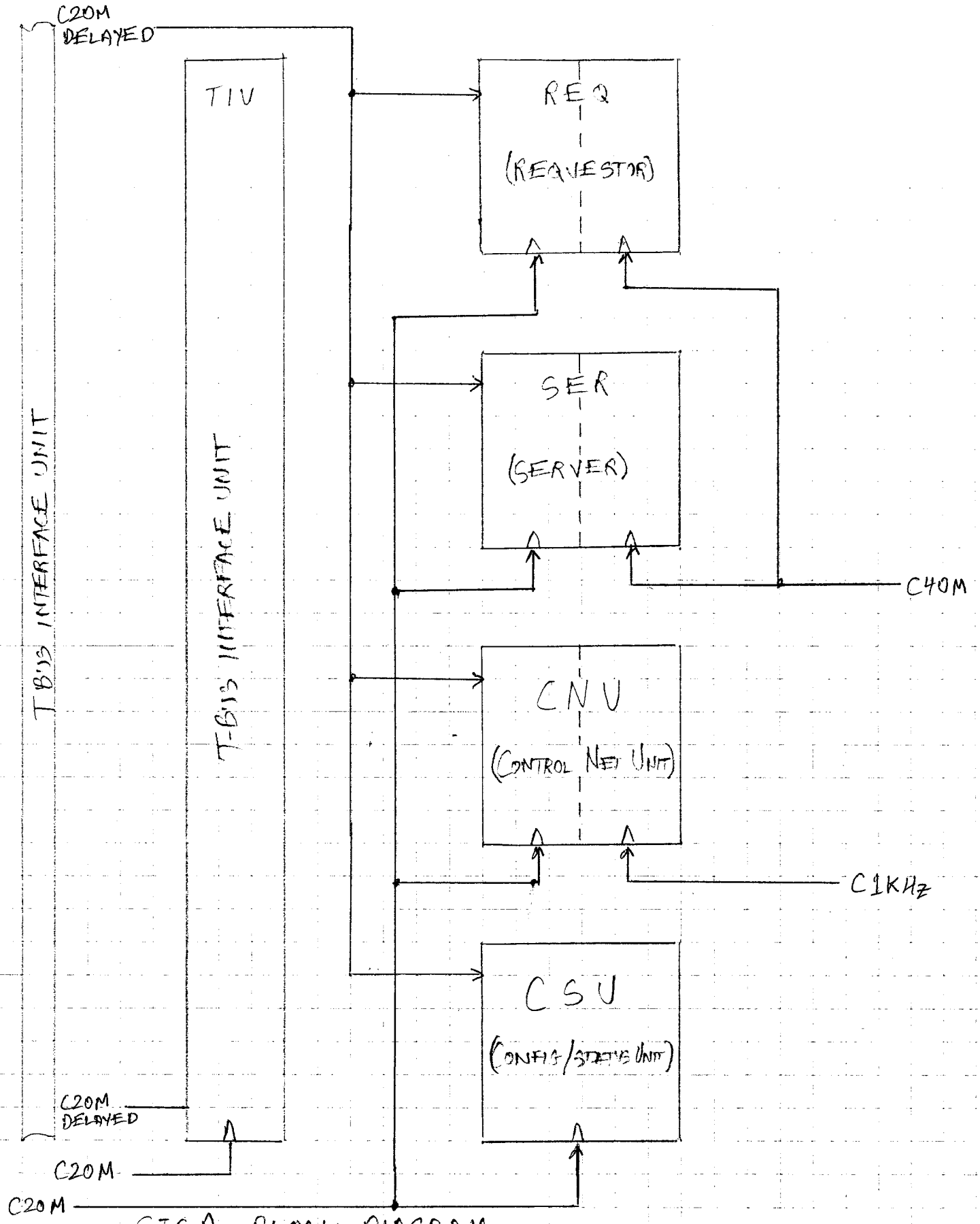
10/8/87 CPL



SIGA BLOCK DIAGRAM

INTERCONNECT

10/8/87CPL



SIGA BLOCK DIAGRAM

CLOCKING

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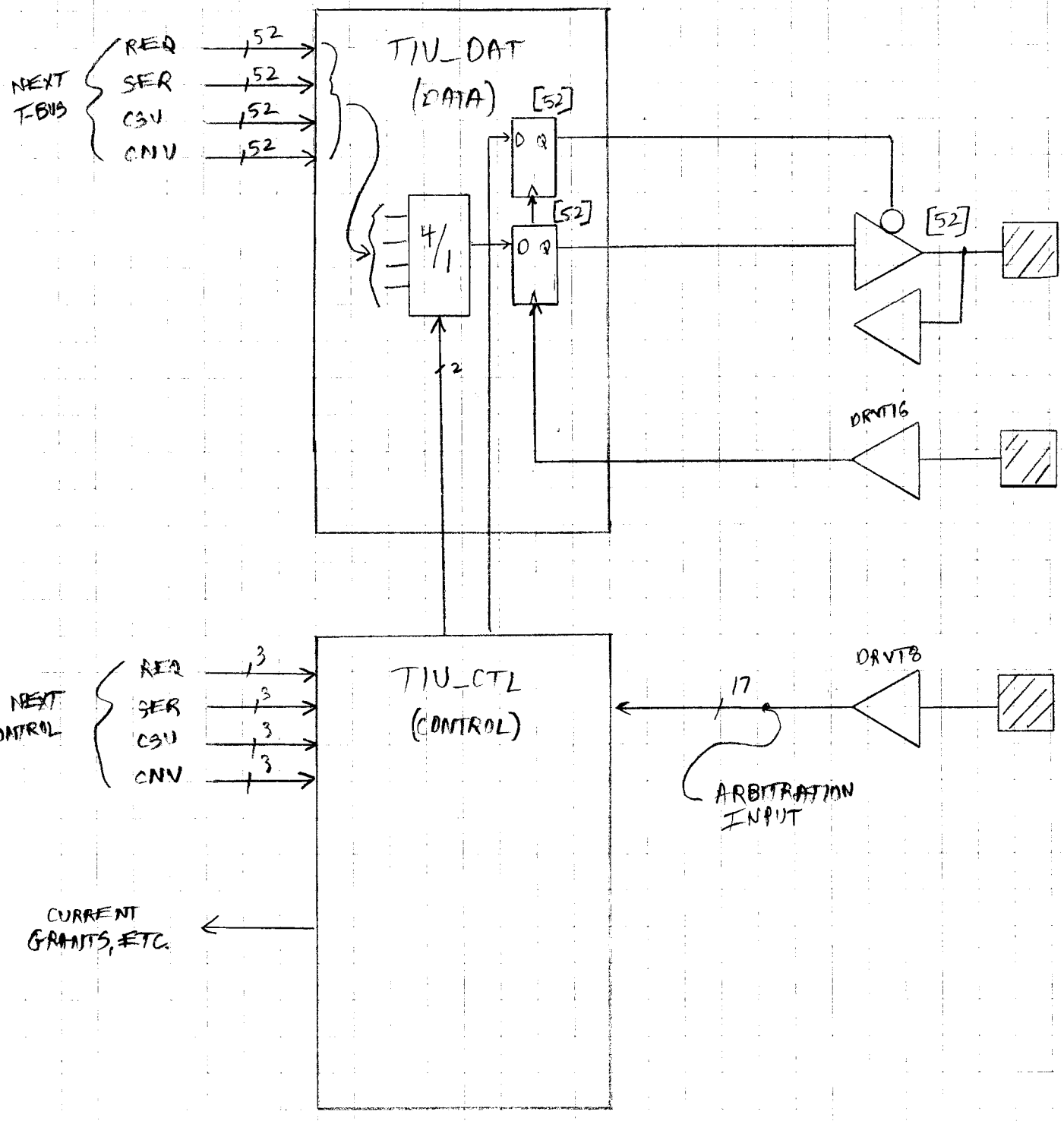

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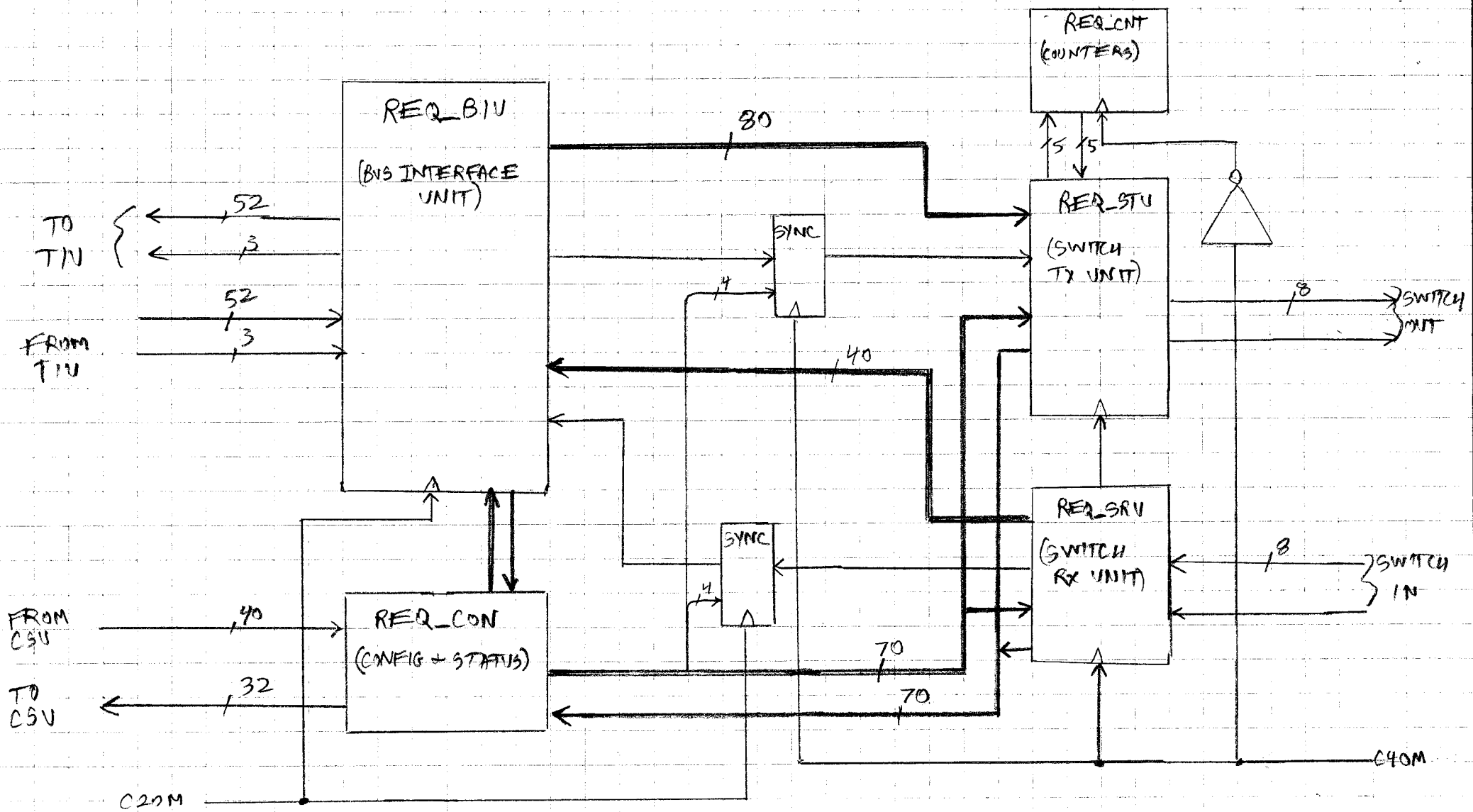
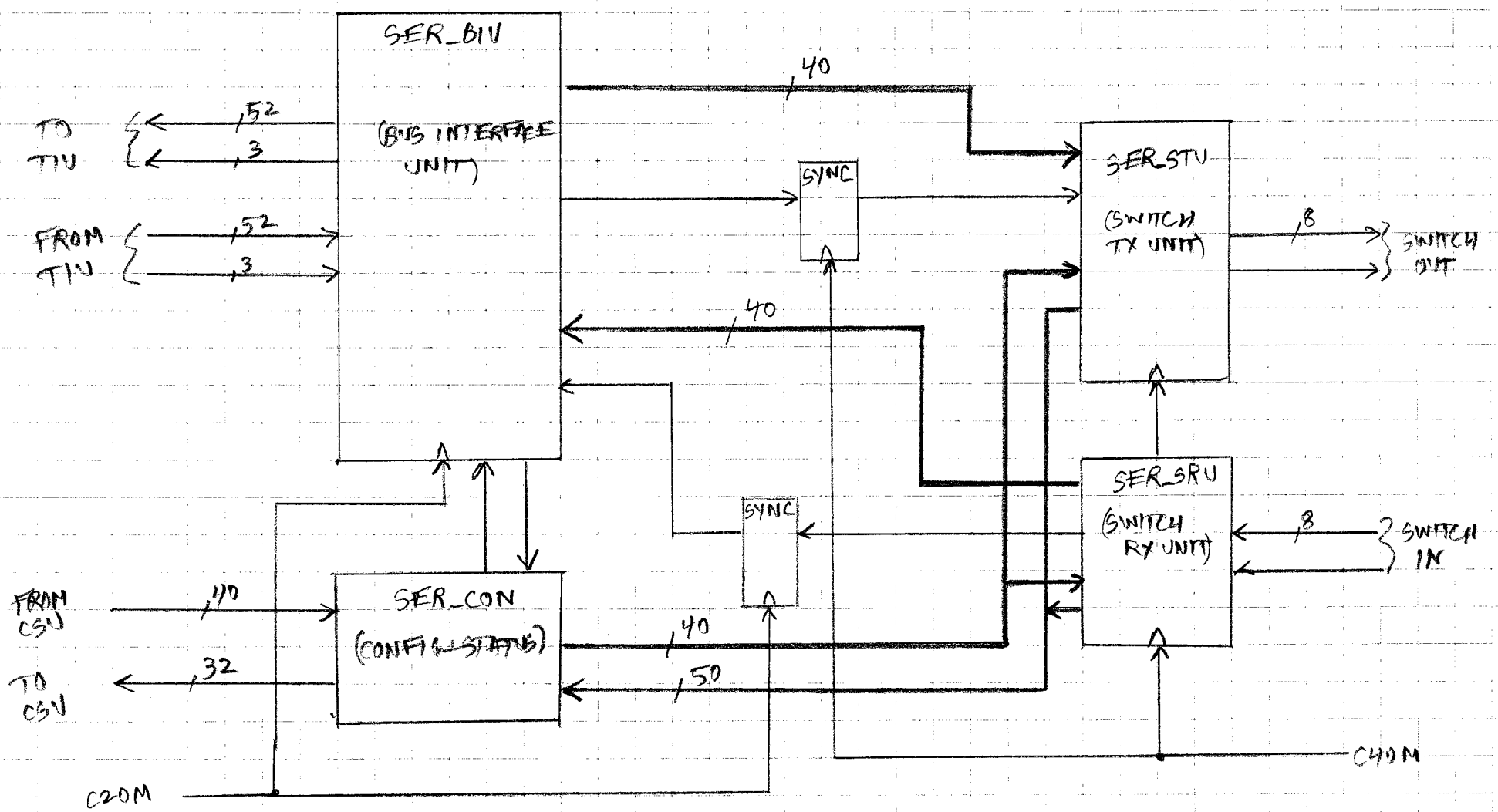
10/2/87 CPL



REQ BLOCK DIAGRAM

10/8/87 CPL



SER BLOCK DIAGRAM

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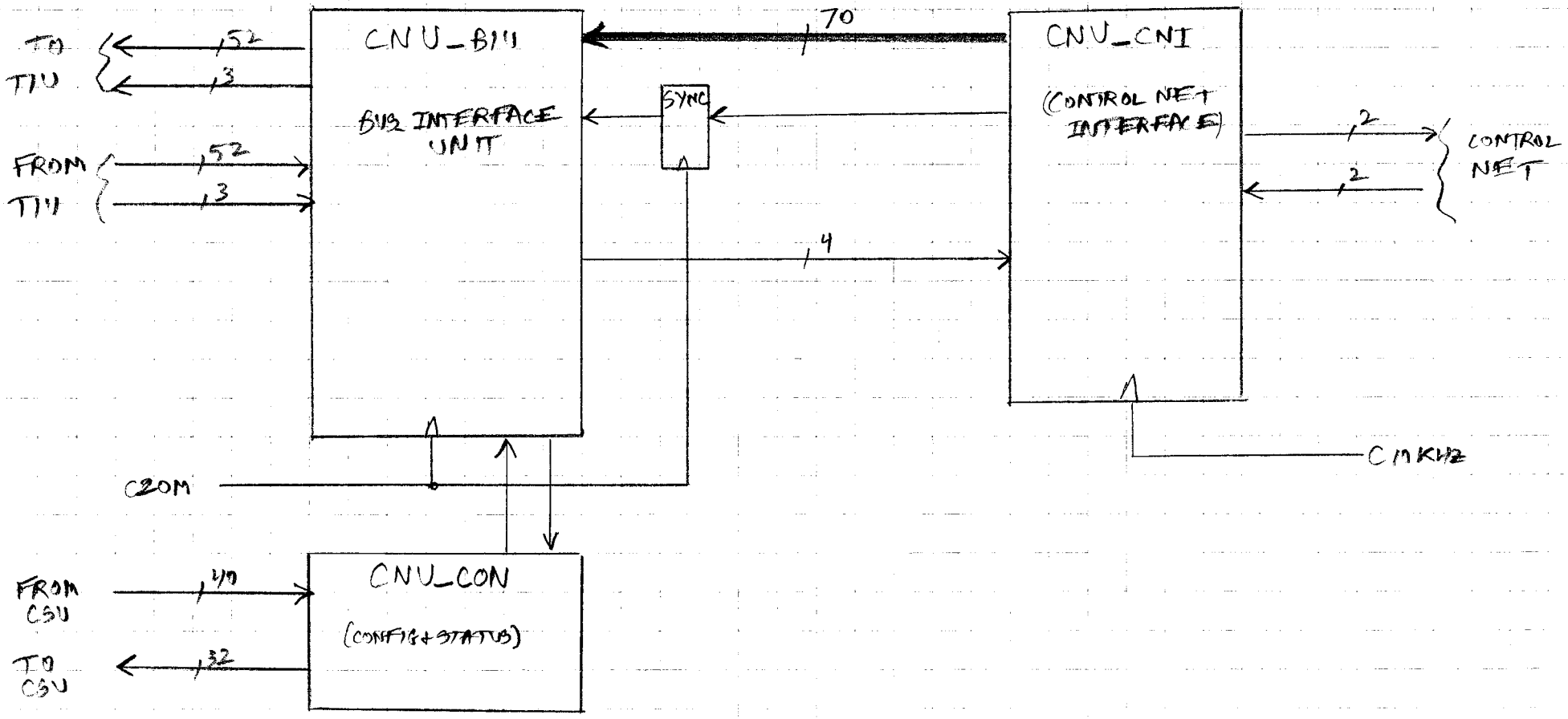
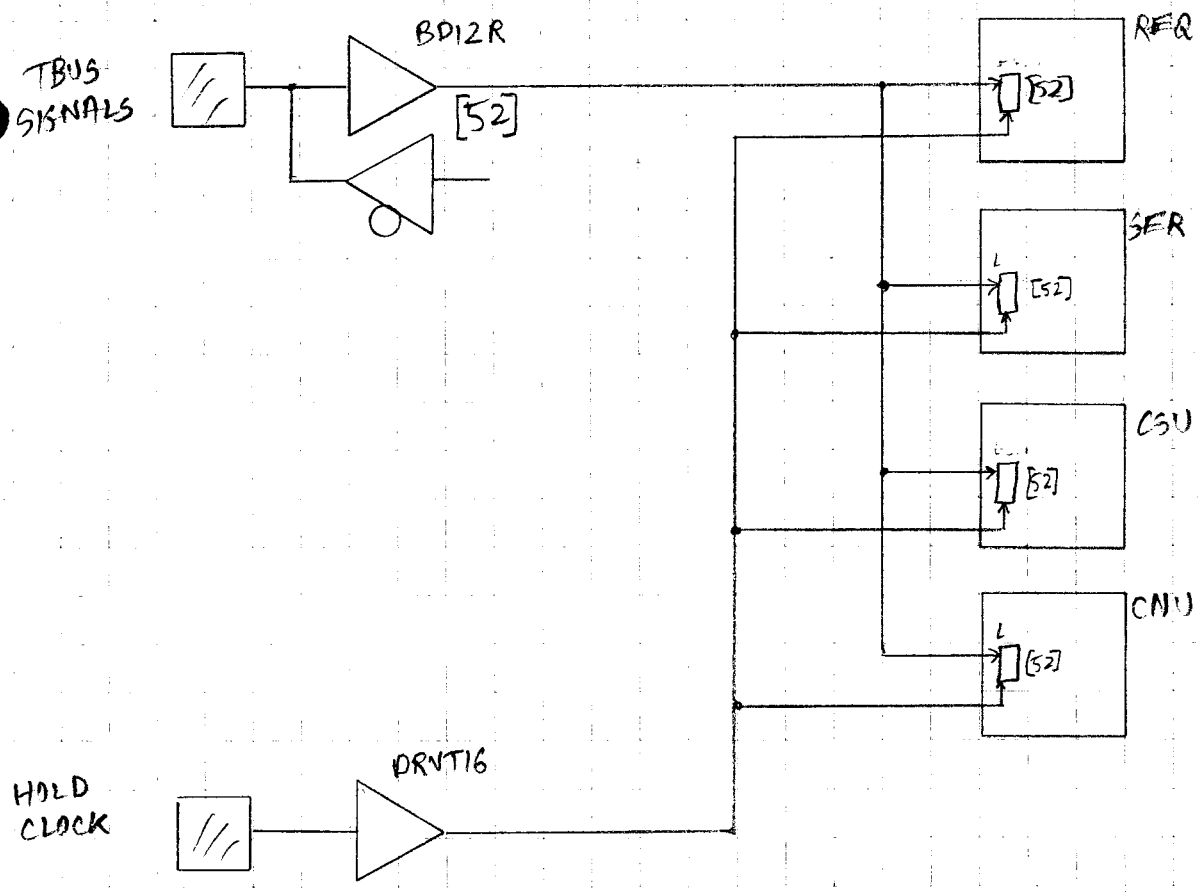
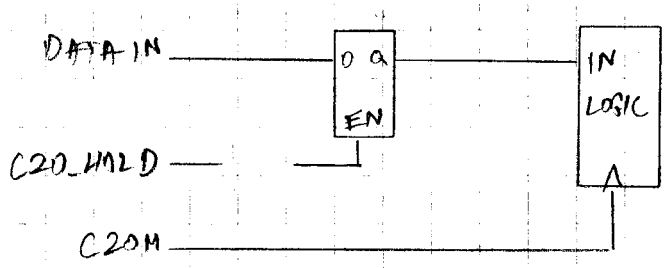
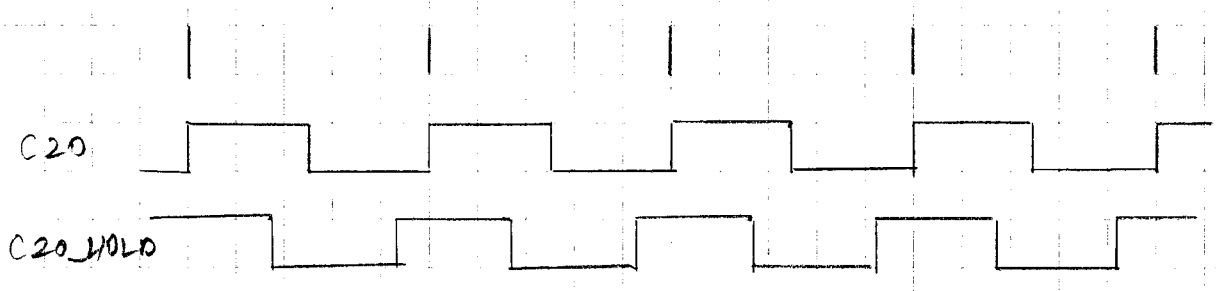


CNU BLOCK DIAGRAM

10/8/87 CPL

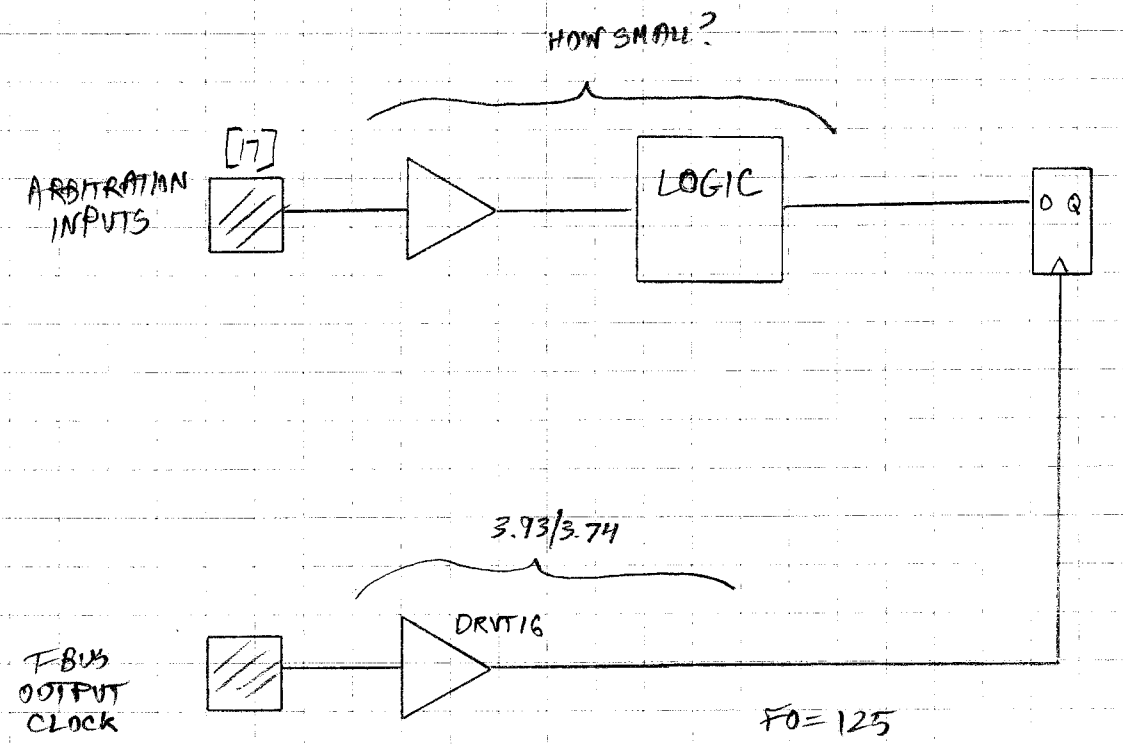






TB'S INPUT HOLD SCHEME

10/8/87 CPL

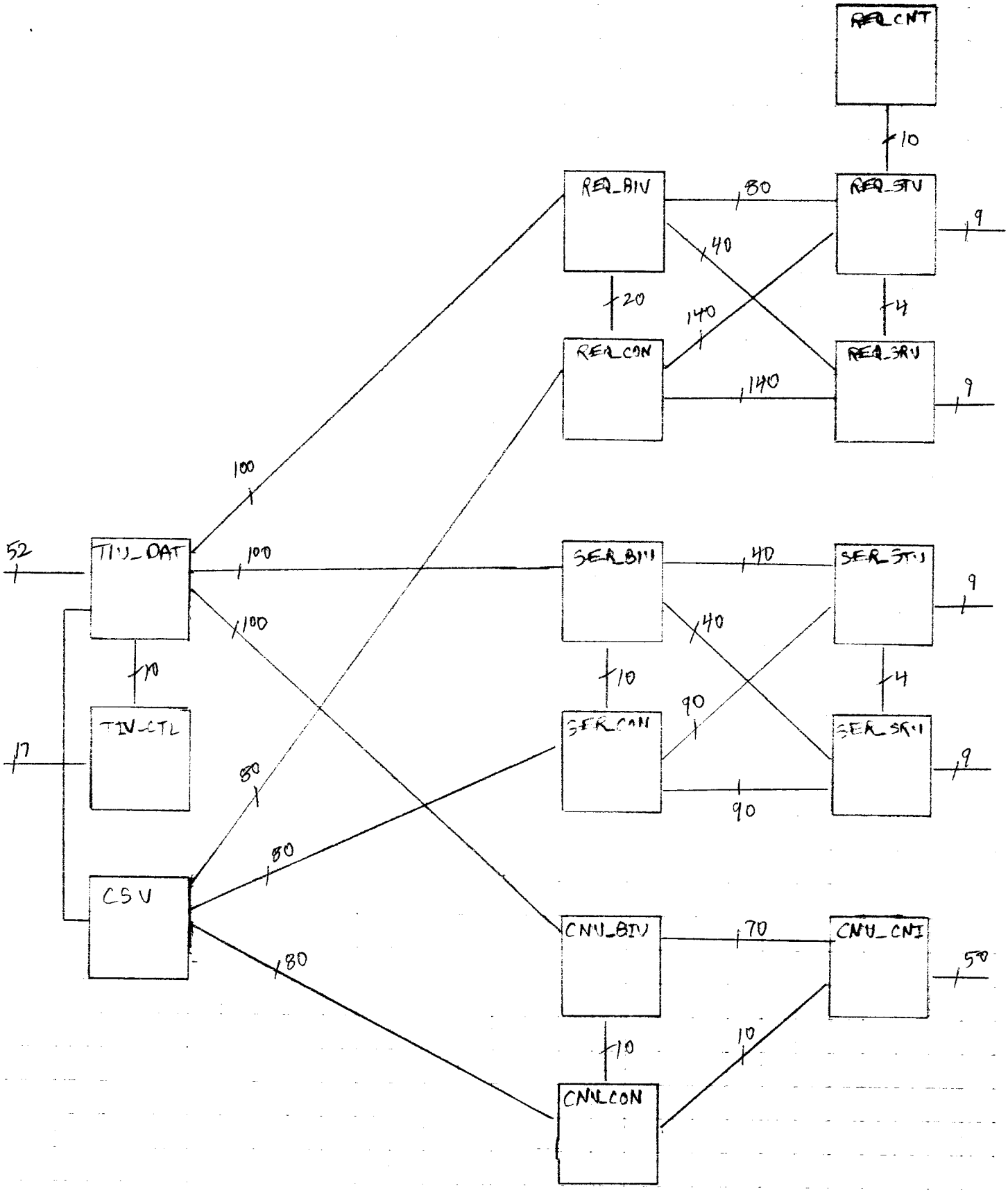


FO=125

E 222/197/125

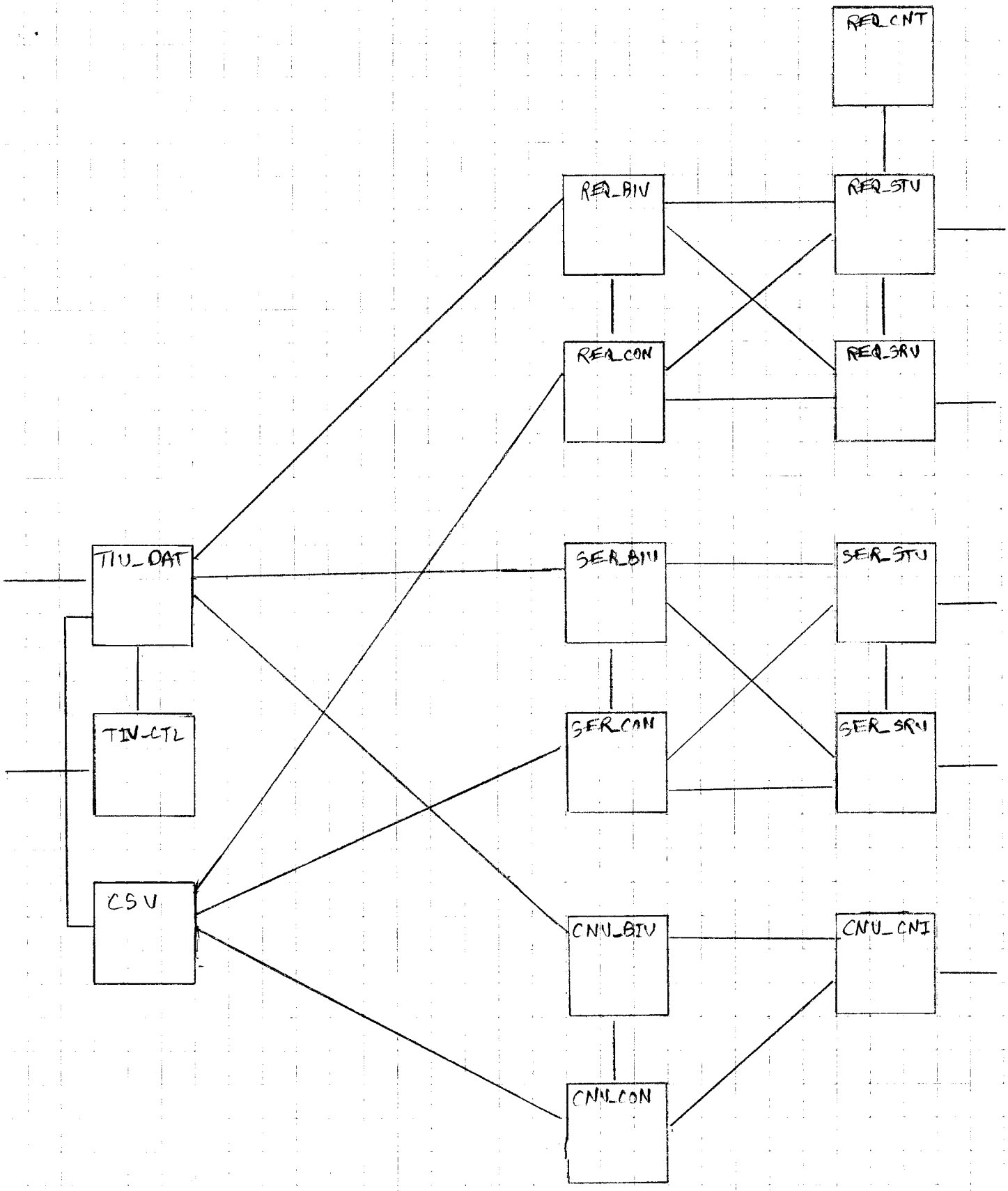
HOLD TIME FEASIBILITY MODEL

10/8/87 CPL



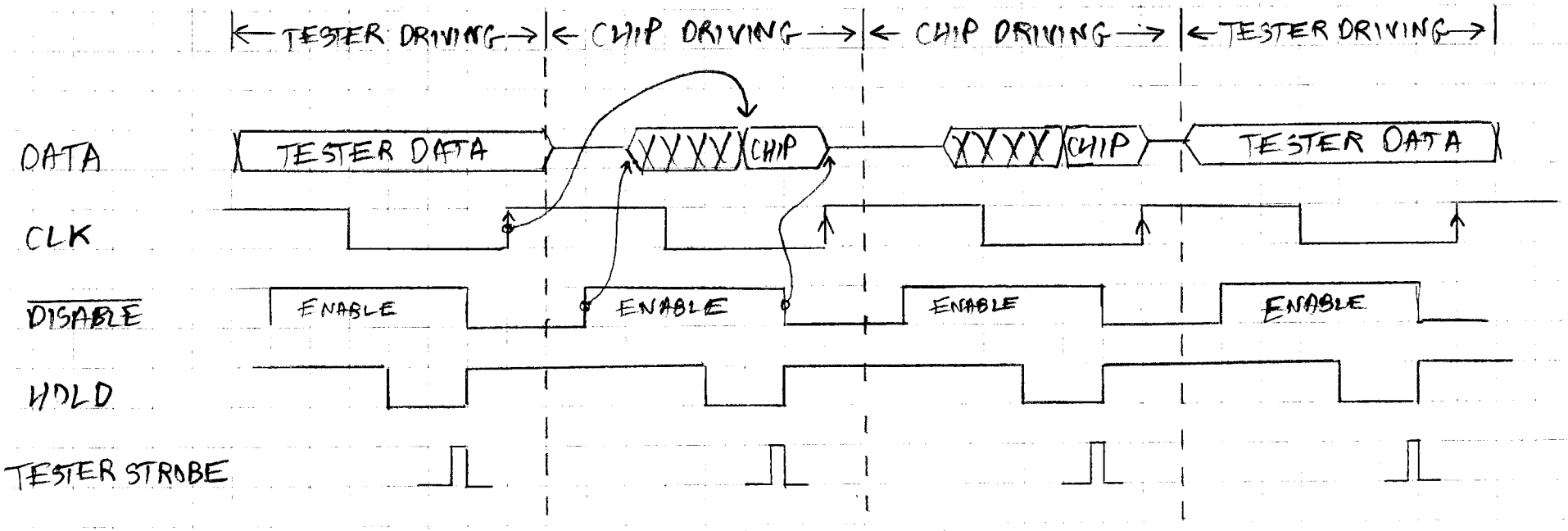
SIGA TOP LEVEL BLOCK INTERCONNECT (ESTIMATED)

10/3/87 CPL

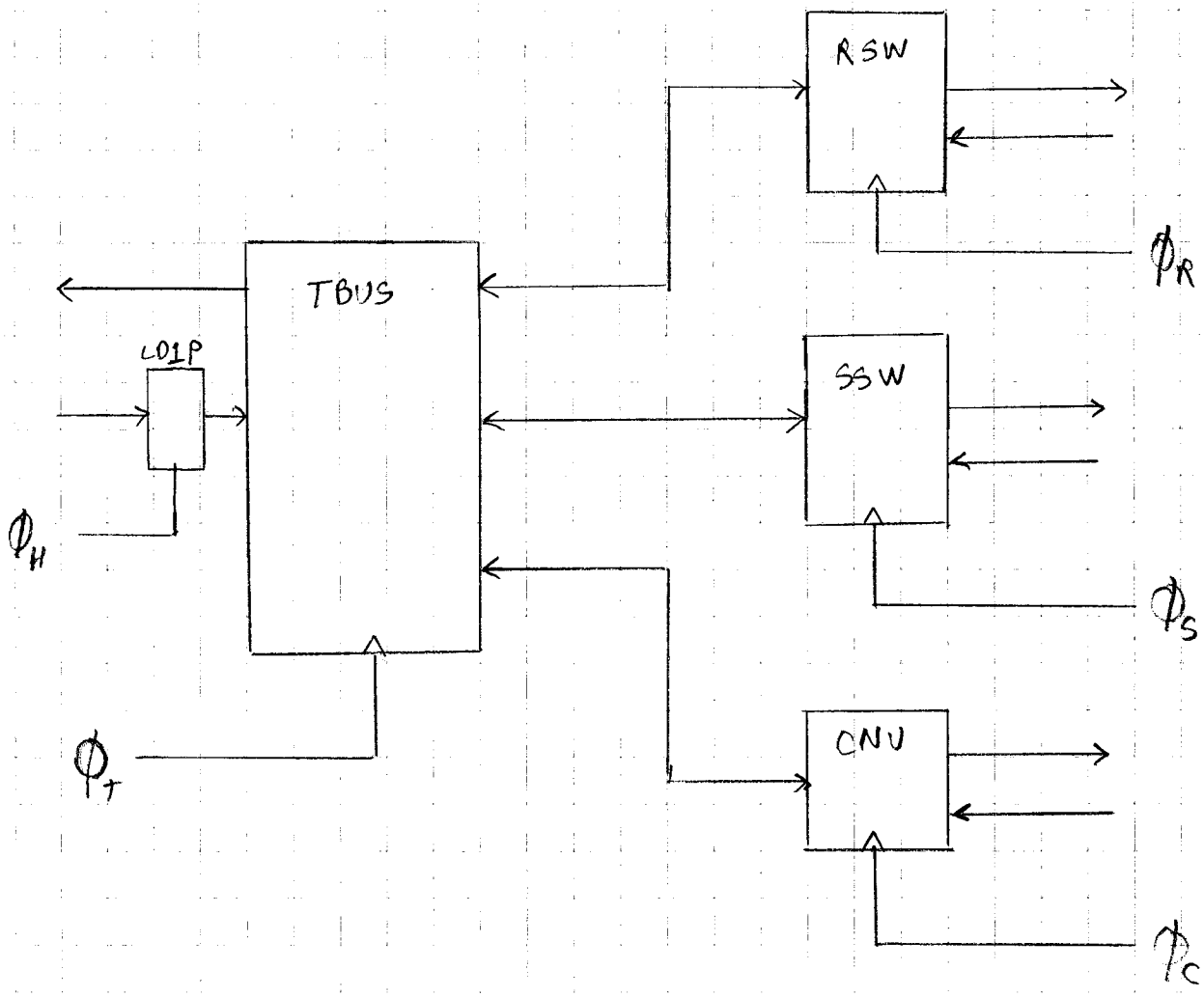


SIGA TOP LEVEL BLOCK INTERCONNECT

10/8/87 CPL



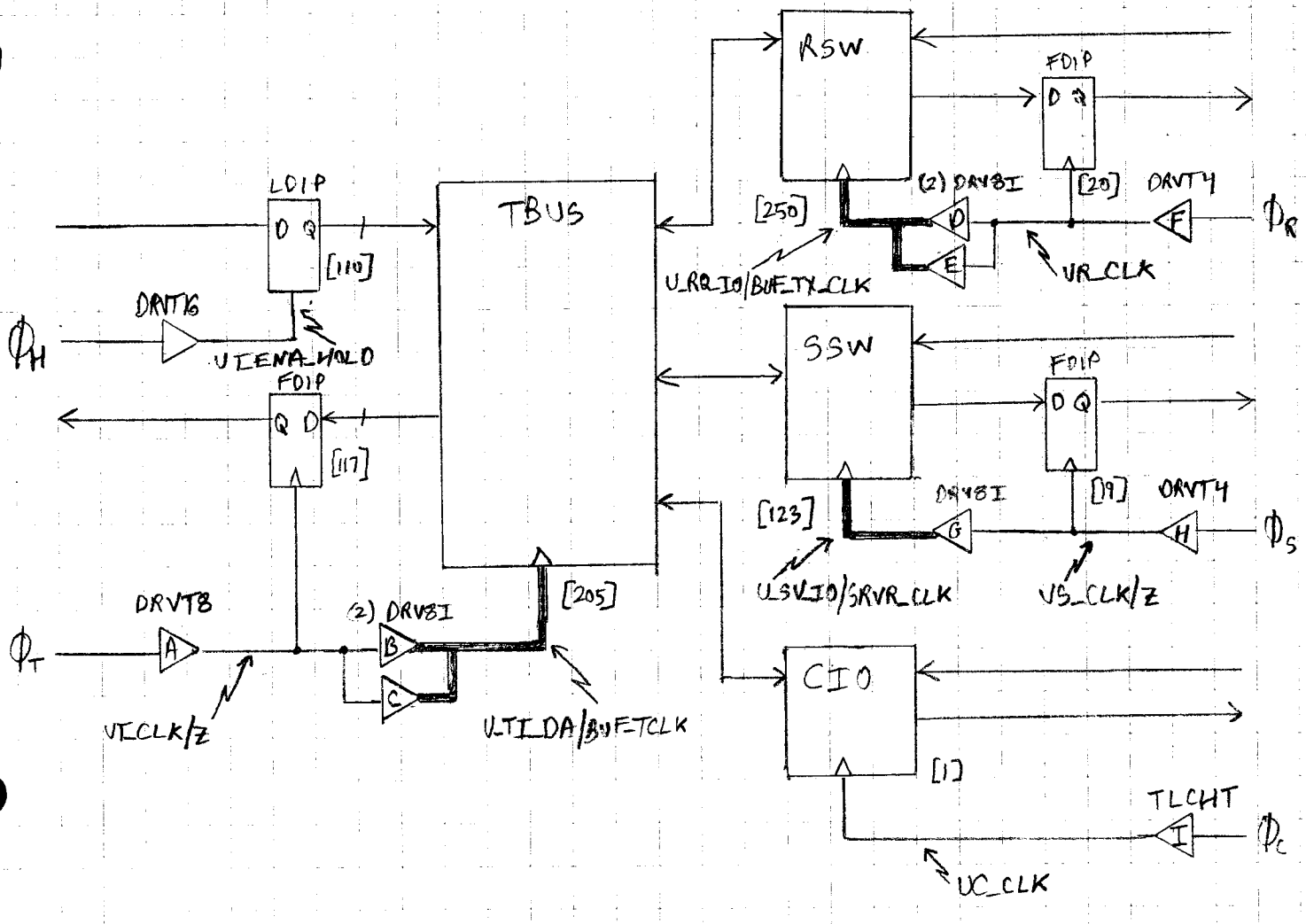
TESTER SCHEME



BLOCK DIAGRAM – CLOCKING SCHEME

FIGURE 1

1/8/87 CPL

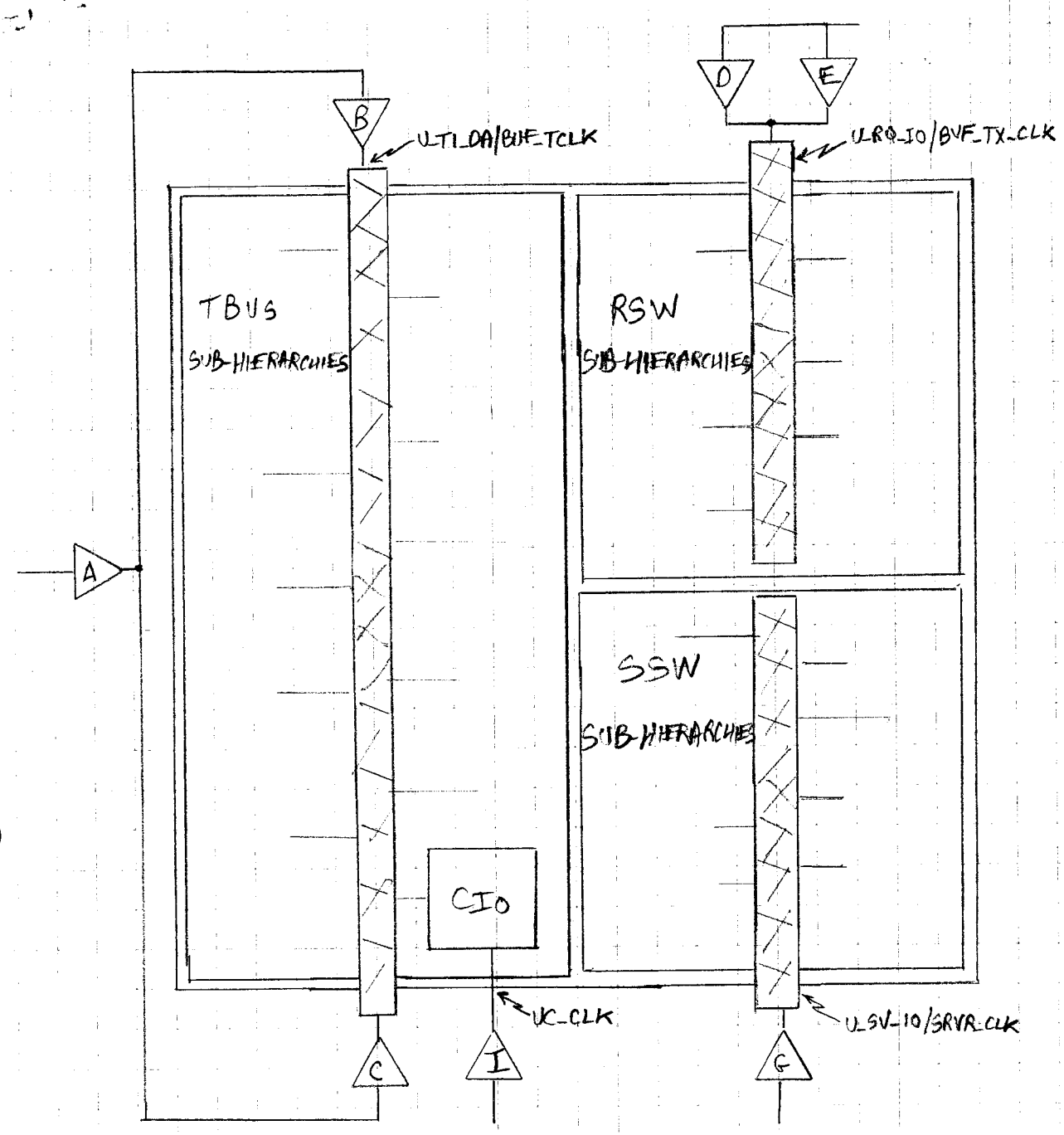


SPECIALLY TREATED CLOCK NETS (INDICATED WITH HEAVY LINES)

SCHEMATIC - CLOCKING SCHEME

FIGURE 2

1/8/88CPL



LAYOUT DIAGRAM - CLOCKING SCHEME

FIGURE 3

1/14/88 PL

PAGE 1 OF 2 PAGES DATE OF TRANSMISSION: 7-29

[redacted]

PRIORITY: ☐ STANDARD ☒ URGENT

STATUS: ☒ STANDARD ☐ CONFIDENTIAL

FACSIMILE MESSAGE

DELIVER TO:

NAME PHIL LEVIN COMPANY BBN

ADDRESS/LOCATION

FAX PHONE 873-3315 OFFICE PHONE 873-2902

SENT BY:

NAME BILL FLETCHER COMPANY LSI LOGIC CORPORATION

ADDRESS/LOCATION 1601 Trapelo Road. Waltham, MA 02154

FAX PHONE 617-890-6158 OFFICE PHONE 617-890-0180

MESSAGE:

07/29/1988 14:03 L.S.I. LOGIC WALTHAM, MA 617 8906158 1470762I P.01

```
    265B2A2A5529  <-- This is last line of current LDSPROF DATA file.
573A3C55370A0C33      Complete as indicated, then add remaining lines of
210C213A23080A1E      code to extend authorization until September 30th.
060B0738230A0706
333A20060B3A0A0D
063A3206330A1E22
3A050C0B3A105B2F
3C39523A5525005A
560F575A5B293A3C
1055005755 2A2855
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575A5B293A3C1055
0057552A2855563A
524A4B4B3C39
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FILE: LATCHUP MEMO A1 * * * L S I L O G I C C O R P., W A L T

Subject: Questionnaire for customers with latch-up problems

LATCH-UP FAILURES OF CMOS PARTS IN THE FIELD

Some of our CMOS parts were destroyed in the field due to latch-up. The parts failed either in testing or in the circuit board. We can find out from the customers if these parts were handled propely by asking them some questions:

1. Is the power supply well regulated at the PC board level? When the power supply is switched on and off, there should not be any voltage overshoot above 7 volts on the power rail, and specifically at the VDD pins of the part. Check the power distribution system on the board. Are there enough by-pass and filtering capacitors?

2. [illegible] customer use in circuit testing? As a good practice, always [illegible]e part in tristate mode before forcing any voltage to the [illegible] of the IC. The forcing voltage should have a current limit [illegible] 100ma maximum. Make sure that the tester pins do not generate any overshoot or ringing voltage 0.7 volts above VDD on the I/O pins of the IC. If there is overshoot, the pulse width should be less than 30ns. Overshoots should be dampened by any means available.

3. Are the parts used in a system where there are tristate buses driven by [illegible] parts? If so, they should see the same ramp time on their V[illegible]. Parts located on separated boards that are powered up at different time will have the greatest chance to be destroyed. This situation should be avoided at all cost, and is one of the main cause of parts failure at the board level.

4. Line reflections and ringings should be kept to minimum. There are TTL tristate drivers capable of sourcing over 100ma. Excessive ringings and overshoot above VDD from these heavy bus drivers can cause damages to the CMOS parts. Check line impedance matching and line termination.

5. A good PC board should be multilayer with solid power and ground planes. This should cut down the output ringings.

Daniel Wong